Research activities on superconducting digital electronics at NICT

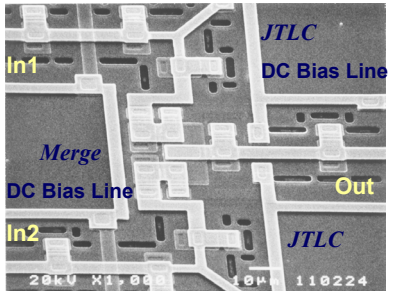
National Institute of Information and Communications Technology

Hirotaka Terai, Shigeyuki Miyajima, Masahiro Yabuno, and Shigehito Miki

R&D of superconducting digital circuits at NICT

NbN-based integrated circuits

Demonstrated the operation of basic SFQ cells and 16-bit shift resister at 9 K



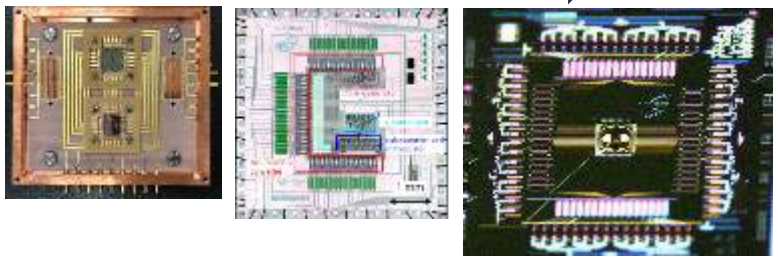
Cell based design for large-scale SFQ circuits

CONNECT
cooperated with SRL, NiCT, NU & YNU

Collaboration between
- ✓ NEC → ISTEC
- ✓ NICT
- ✓ NU
- ✓ YNU

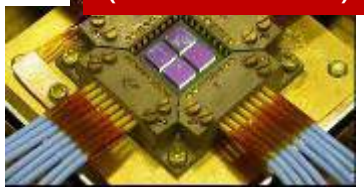
Cryogenic signal processing for SNSPD array

64-pix SNSPD imaging array



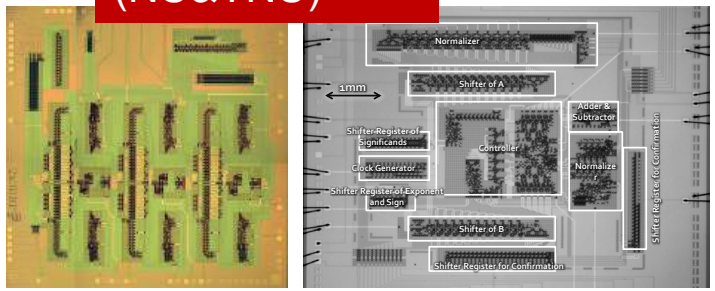
NEDO

4x4 cross-bar switch demo. (ISTEC-SRL)



科研費 KAKENHI

Microprocessor (NU&YNU)



Low-power circuit
- ✓ ERSFQ (Hypres)
- ✓ LV-SFQ, HFQ (NU)
- ✓ RQL (Northrop Grumman)
- ✓ AQFP (YNU)

C3 project in US

Super Tools

IMEC

3 Nb layers 2.5 kA/cm² Standard process (NEC)

4 Nb layers 2.5 kA/cm² Standard process (ISTEC)

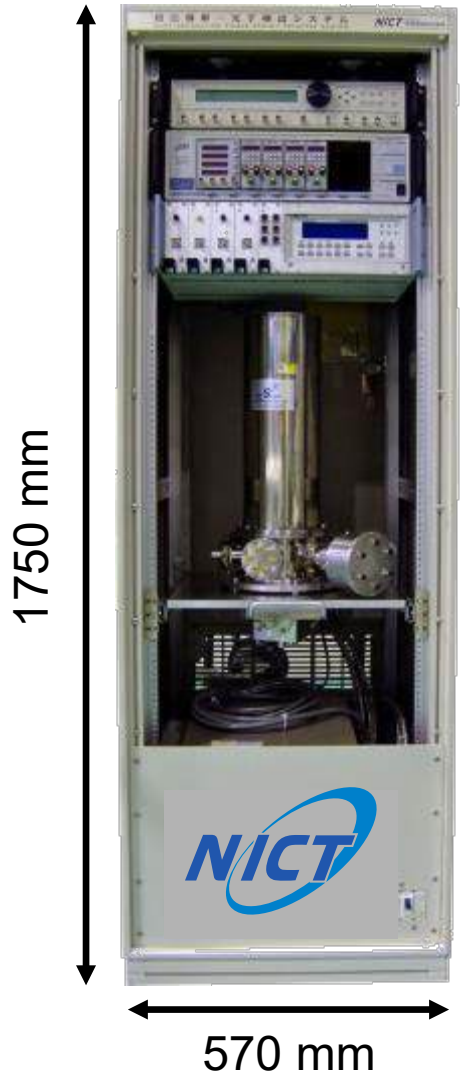
9 Nb layers 10 kA/cm² Advanced process (ISTEC)

CRAVITY AIST

Qufab

1998 2000 2010 2020

Multi-channel SNSPD system

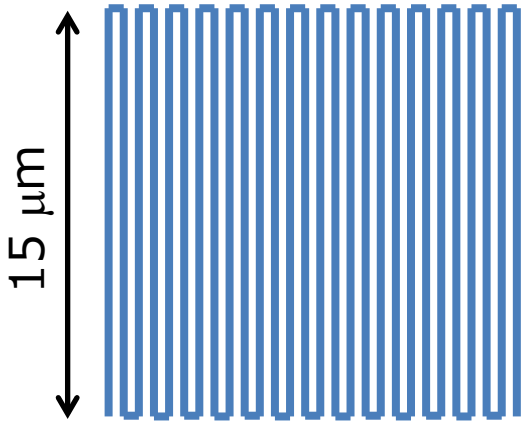


	Typical	Unit
System DE (λ=1550 nm)	90	%
Dark Count Rate	1-100	cps
Maximum Count Rate	20-40	MHz
Jitter (FWHM)	50	ps
Input	Opt. fiber (SMF or MMF)	----
Output port	SMA	----
Cryocooler	0.1 W GM (Air cooling、AC100V)	----
Lowest Temp.	< 2.5	K
Operation time	10,000	hours

There are seven startups selling SNSPD systems worldwide

Multi-pixel SNSPD

Single pixel



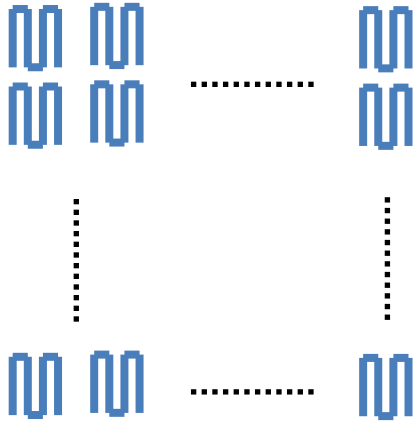
Nanowire length : ~ 1 mm

Kinetic inductance L_K ~ 1 μH

Dead time : L_K/50 Ω ~ 20 ns

Maximum count rate : ~ 50 MHz

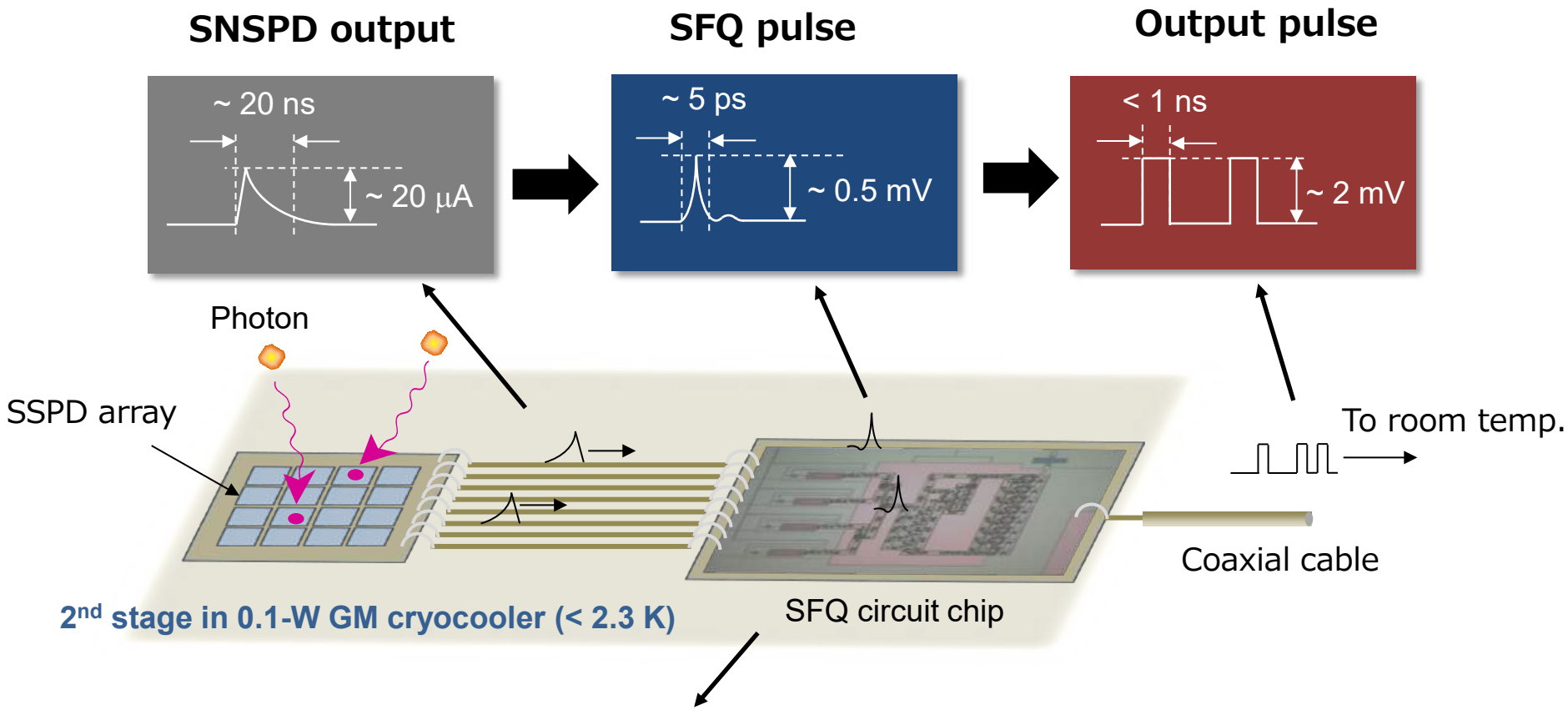
Multi-pixel



Reduction of L_K

- ✓ High speed, large area
- ✓ Photon-number resolution
- ✓ Single-photon imaging

Post signal processing using SFQ circuit for multi-pixel SNSPD



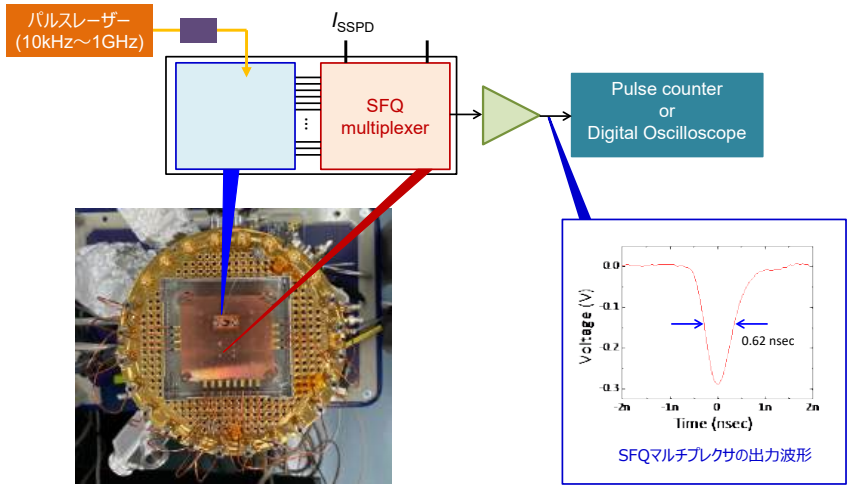
Various signal processing using SFQ circuits

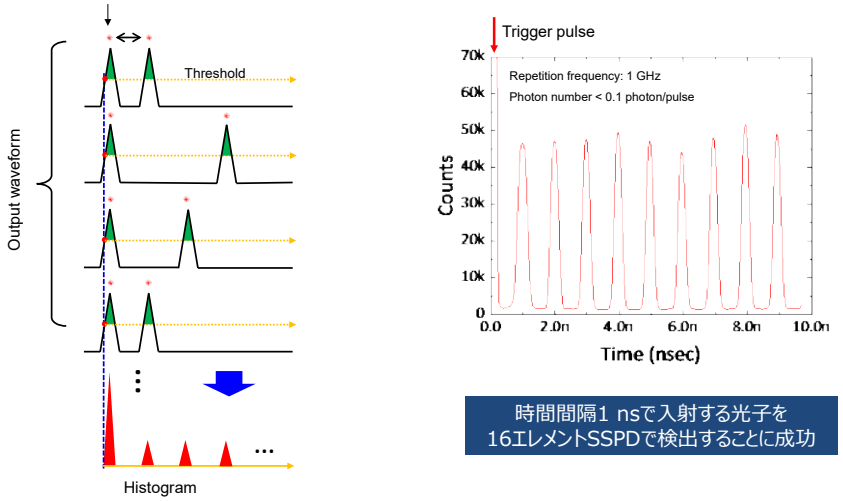
- ✓ Multiplexing
- ✓ Pseudo photon-number resolution
- ✓ Address encoder for single-photon imaging
- ✓ High-time-resolved coincidence detection

H. Terai *et al.*, *IEEE TAS* **19**, 350-353 (2009)

Achievements using SFQ signal processor

Single-photon detection with 1-ns time interval





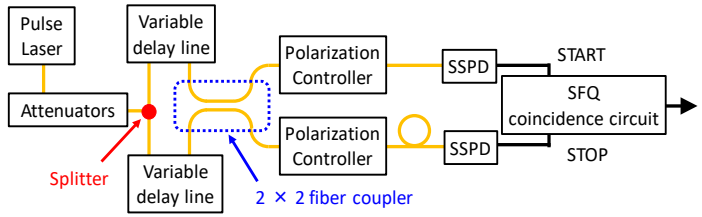
時間間隔1 nsで入射する光子を
16エレメントSSPDで検出することに成功

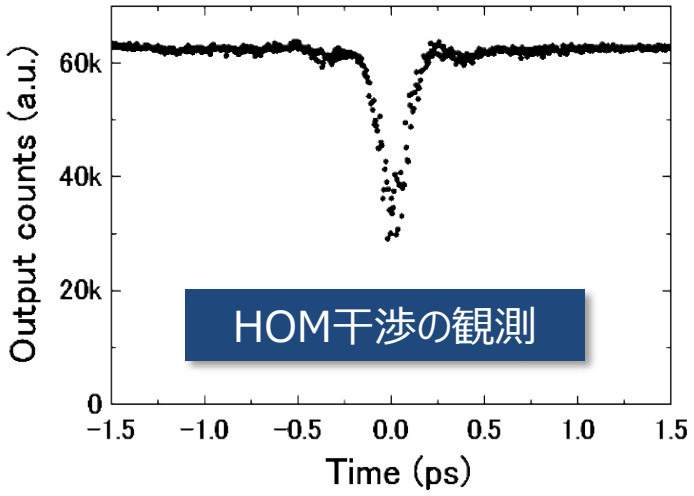
S. Miki *et al.*, Opt. Lett., **46**, 6015 (2021)

Coincidence detection

Time resolution of coincidence detection

- ✓ TCSPC module (Hydra harp 400): 68.3 ps
- ✓ **SFQ coincidence detector: 32.3 ps**



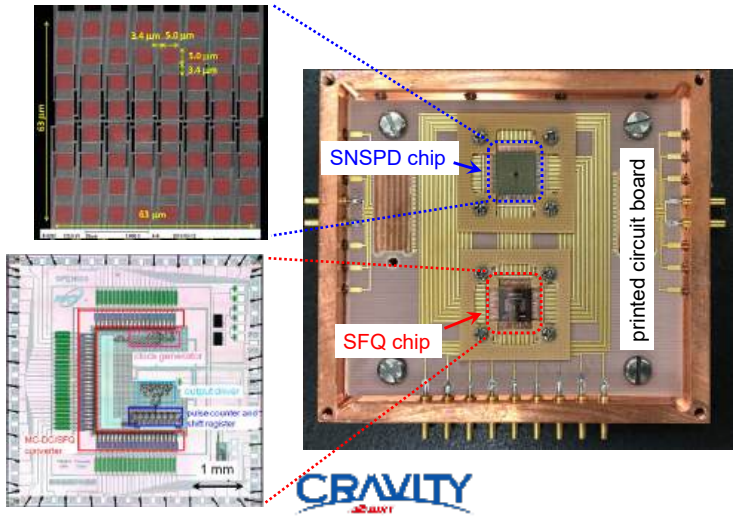


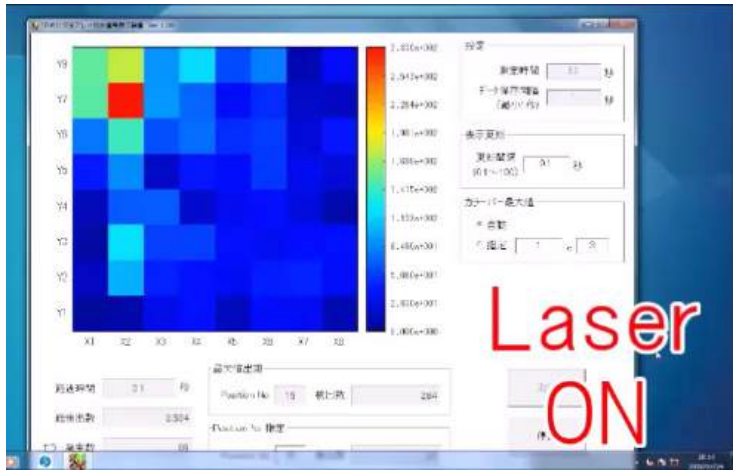
S. Miyajima, *et al.*, Supercond. Sci. Technol., **30,** 12LT01 2017

S. Miki *et al.*, Appl. Phys. Lett., **112**, 262601 (2018)

Achievements using SFQ signal processor

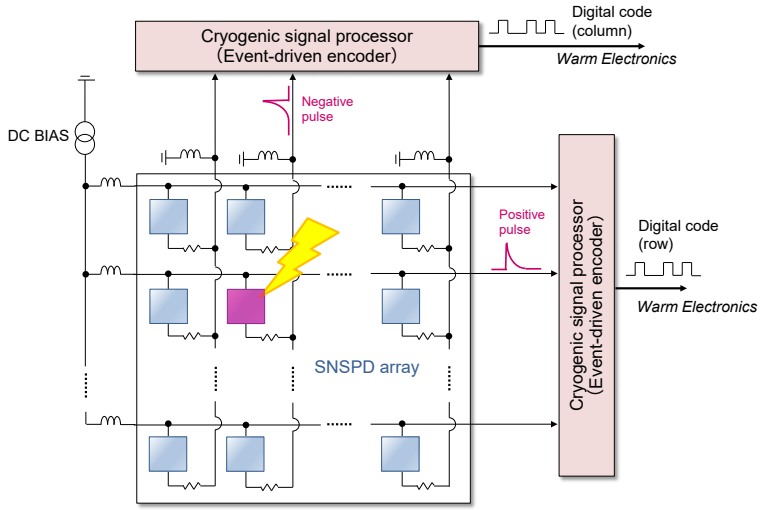
64-pix SNSPD imager

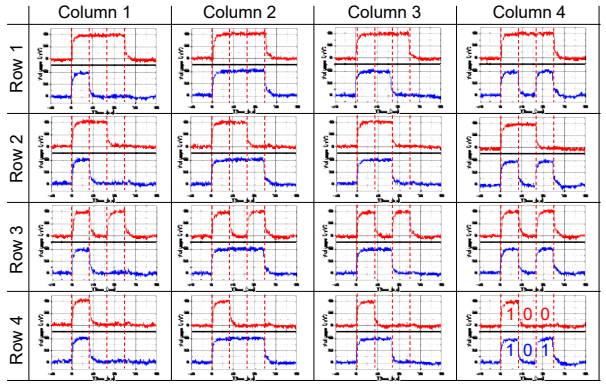




S. Miyajima *et al.*, *Optics Express* **26**, 29045 (2018)

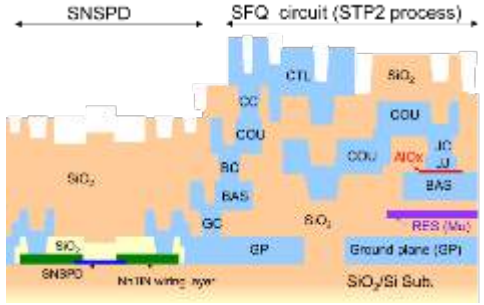
4x4 row-column imager

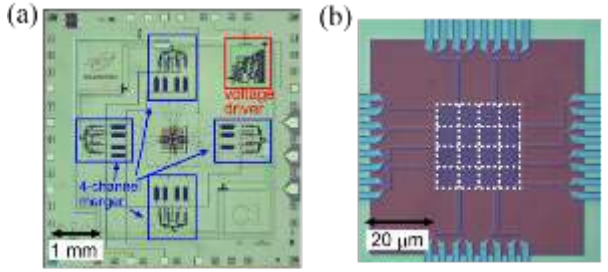


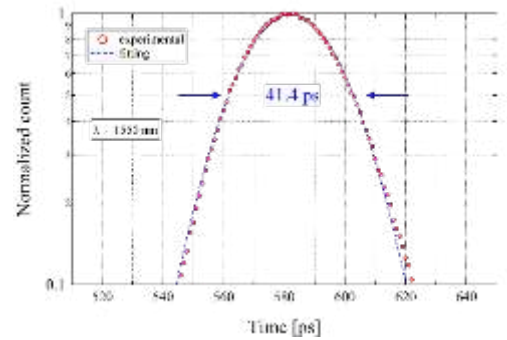


M. Yabuno *et al.*, *Optics Express* **28**, 12047, 2020

Monolithic integration of SNSPD and SFQ circuit







S. Miyajima *et al.*, Appl. Phys. Lett., **112**, 182602 (2023)

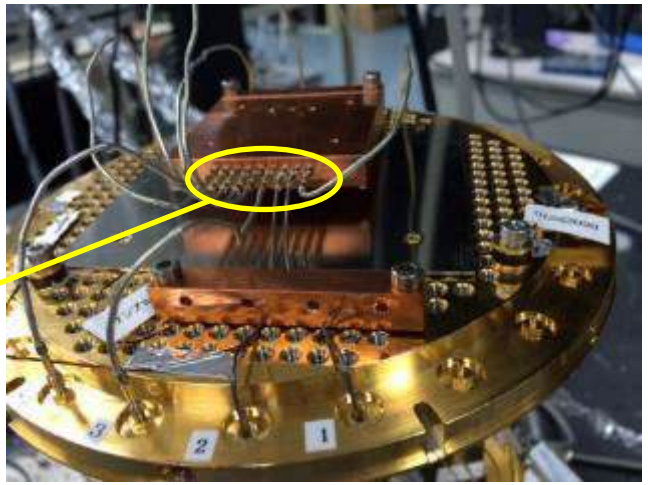
Implementation of SFQ circuit to a cryocooler

Temperature rise（Sumitomo 0.1 W GM cryocooler RDK-101 ）	
Catalog spec. : 0.006 K/mW → 0.6 K/0.1 W	Experiment : 0.044 K/mW **0.1 K/mW near the heat source**

Allowable heat generation at 2nd stage → 5 mW

If the bias line connector has a contact resistance of **20 mΩ**, a bias current of **0.5 A** will generate joule heating of **5 mW**.

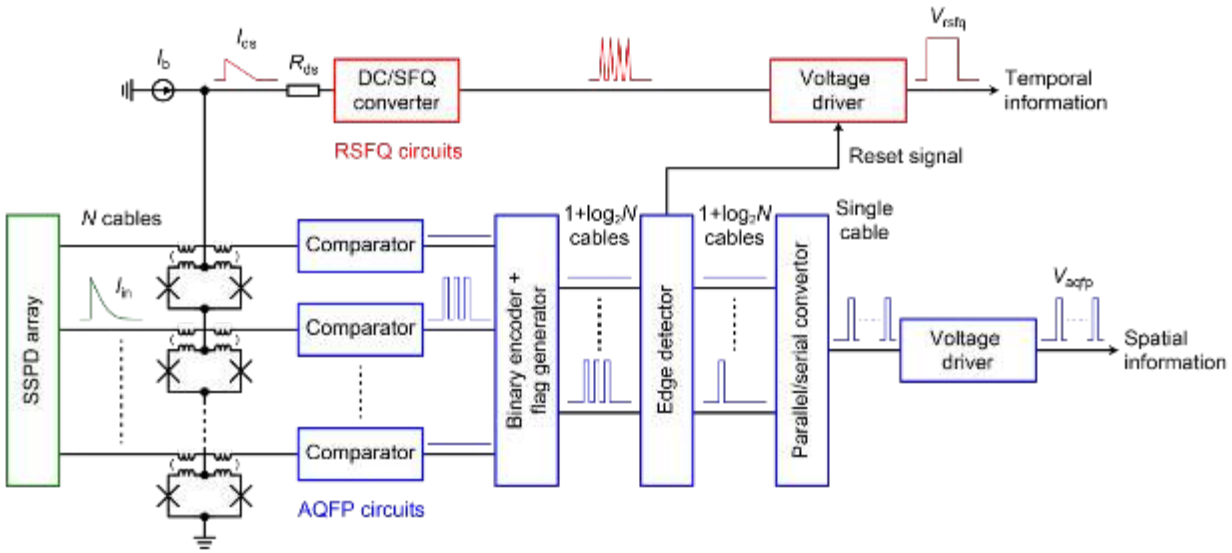
Miniature connector for 65-GHz RF signal manufactured by Kawashima Inc.

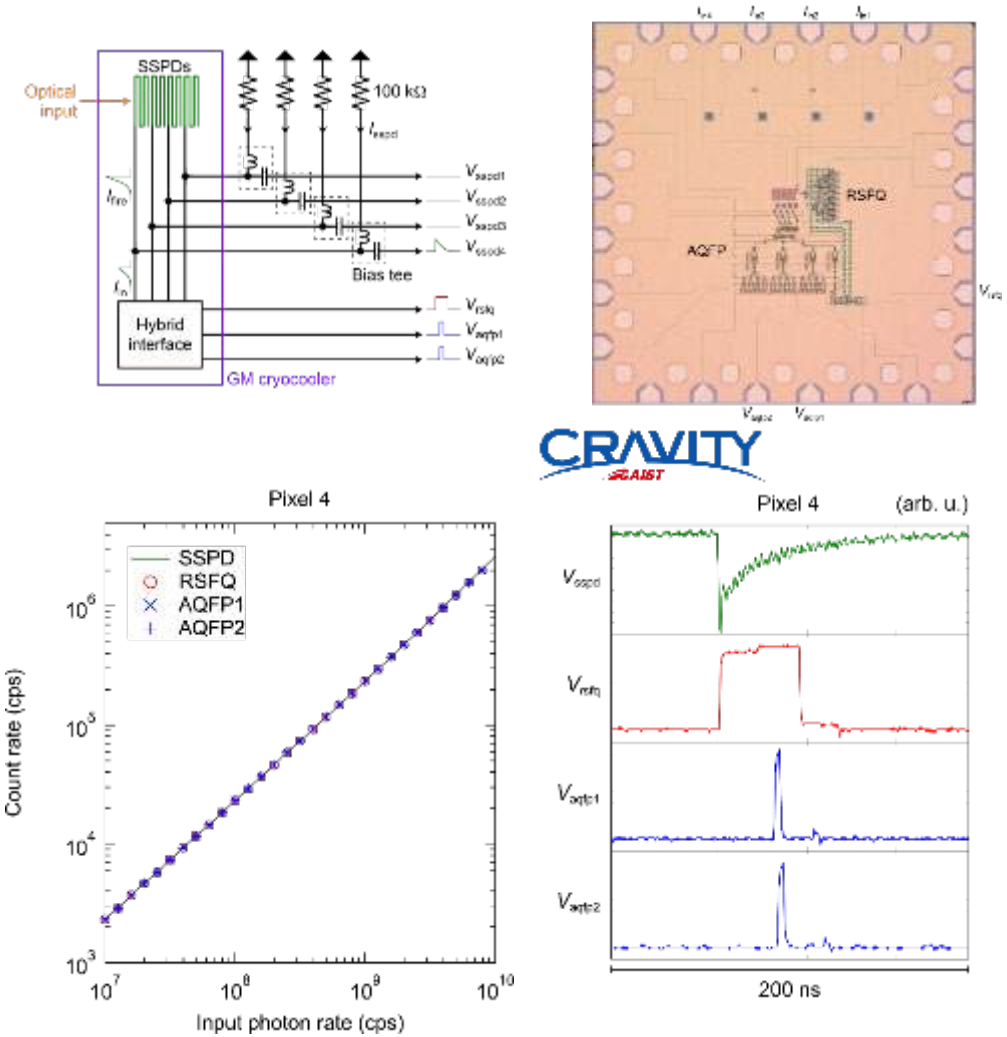


Solutions

- ✓ Use a circuit that can be driven by less current such as AQFP
- ✓ Use the connector with low contact resistance specialized for dc current supply

AQFP/SFQ hybrid encoder



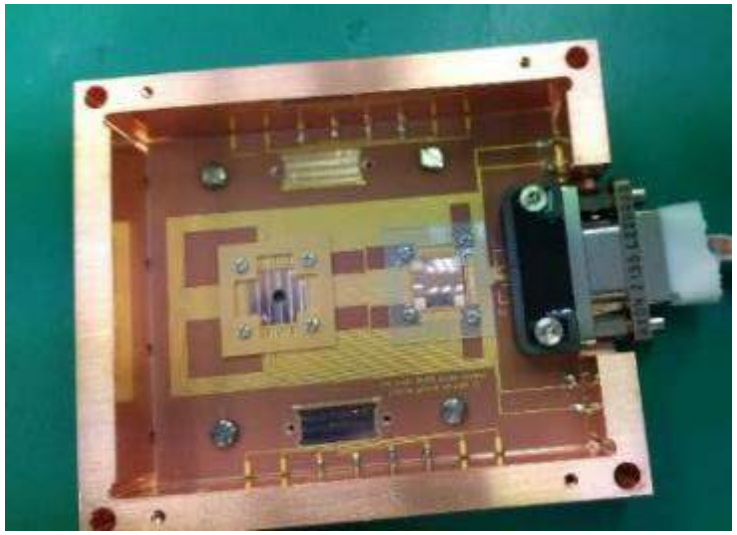


- ✓ The time information of photon detection is readout through SFQ circuit with low timing jitter.
  → Bias current to the SQUID is kept constant independent of the number of input channels.
- ✓ Spatial information of photon detection is readout through AQFP circuit.

*Collaborating with YNU and AIST

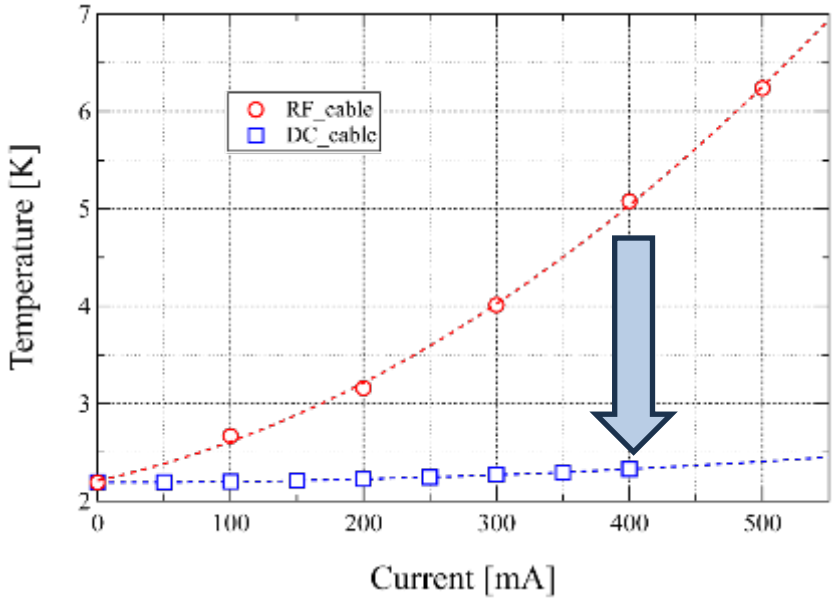
N. Takeuchi *et al.*, *IEEE TAS* **29**, 2201004, 2019
N. Takeuchi *et al.*, *Optics Express* **28**, 15824, 2020

Dc bias current supply via μ-Dsub connector

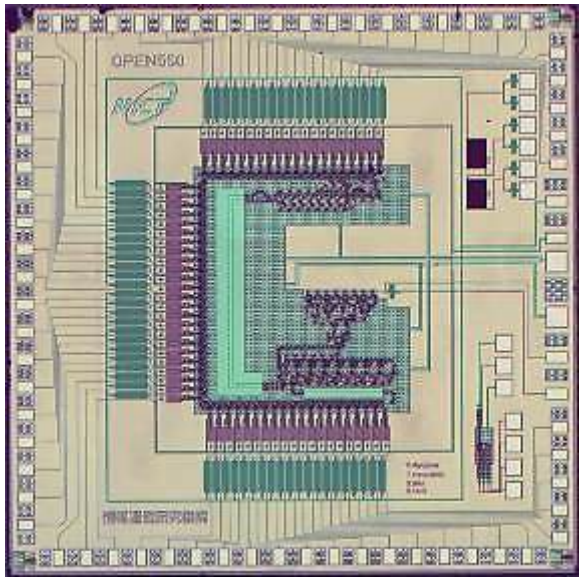


Non-magnetic (<20 nT)
μ-Dsub Connector

Contact resistance: 0.376 mΩ @ 2.4 K



Temperature rise due to dc current supply can be suppressed by using μ-Dsub connector



64-ch event driven encoder

- ✓ Minimum I_c: 100 μA
- ✓ # of JJ: 2610
- ✓ Bias current: 270 mA

Bias Margin: 198 mA – 248 mA
Temperature rise: 0.1 K

Miyajima et al., 70th JSAP spring meeting

Difficulties unique to superconducting digital circuits

- ✓ **Debugging is difficult after cooling.**

  Difficult to identify the origin and location of the errors.

  → Difficult to provide feedback to the design and fabrication process.

- ✓ **Not only circuit defects but also trapped flux can cause malfunctions.**

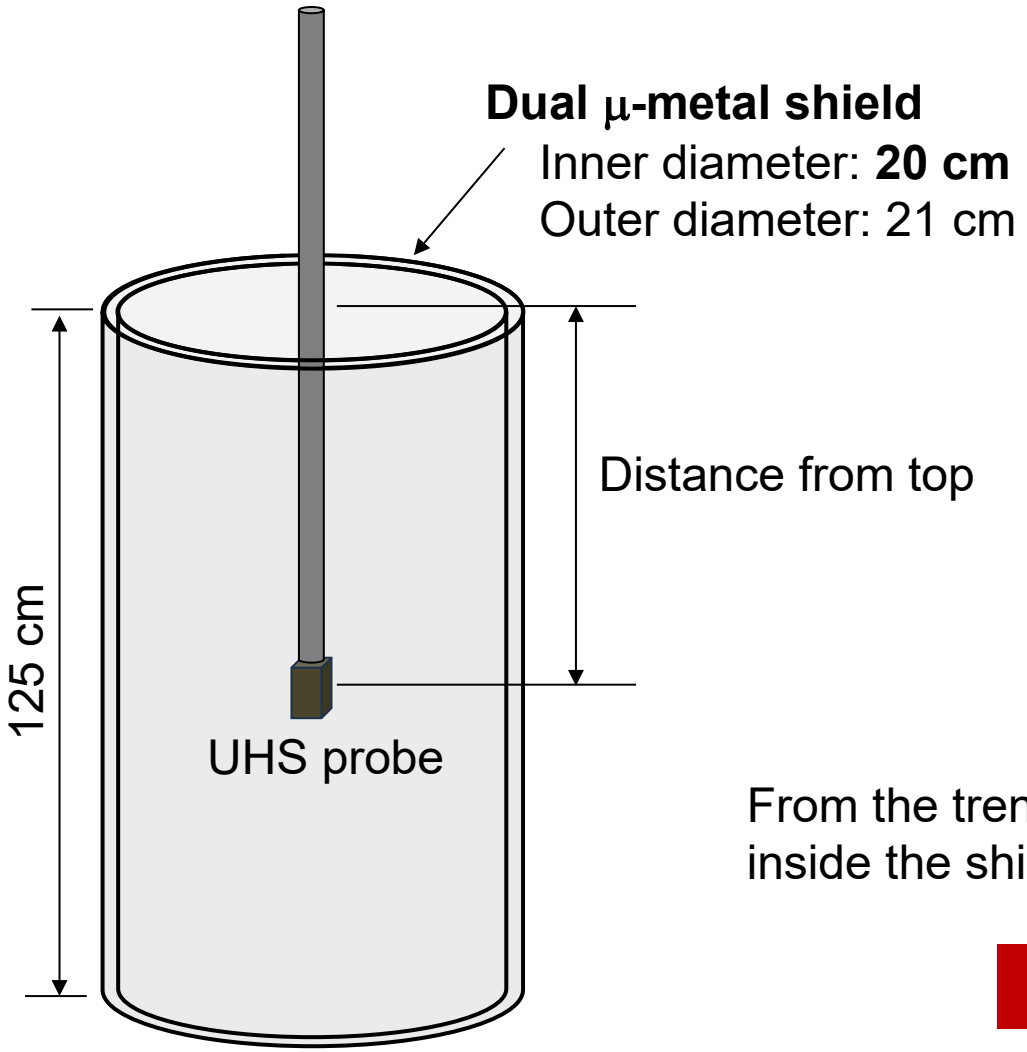
  Moat in GP is not a perfect solution to eliminate the effect of trapped flux.

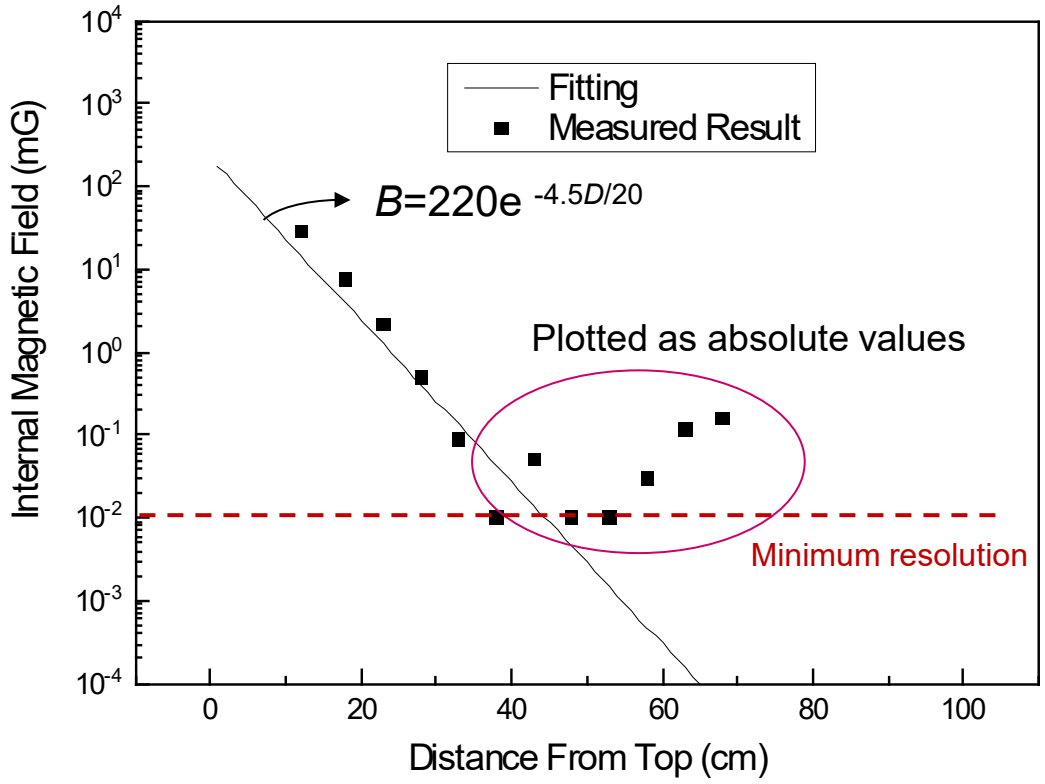
Possible sources of flux trapping

- ✓ Residual magnetic field due to insufficient magnetic shield
- ✓ Magnetization of μ-metal shield
- ✓ Magnetization of screws and other parts around the chip
- ✓ Thermoelectric current due to Seebeck effect
- ✓ External noise

Residual magnetic field in the dual μ-metal shields

LakeShore Type-421 Gaussmeter＋UHS probe → **Measurement resolution：0.01 mG**





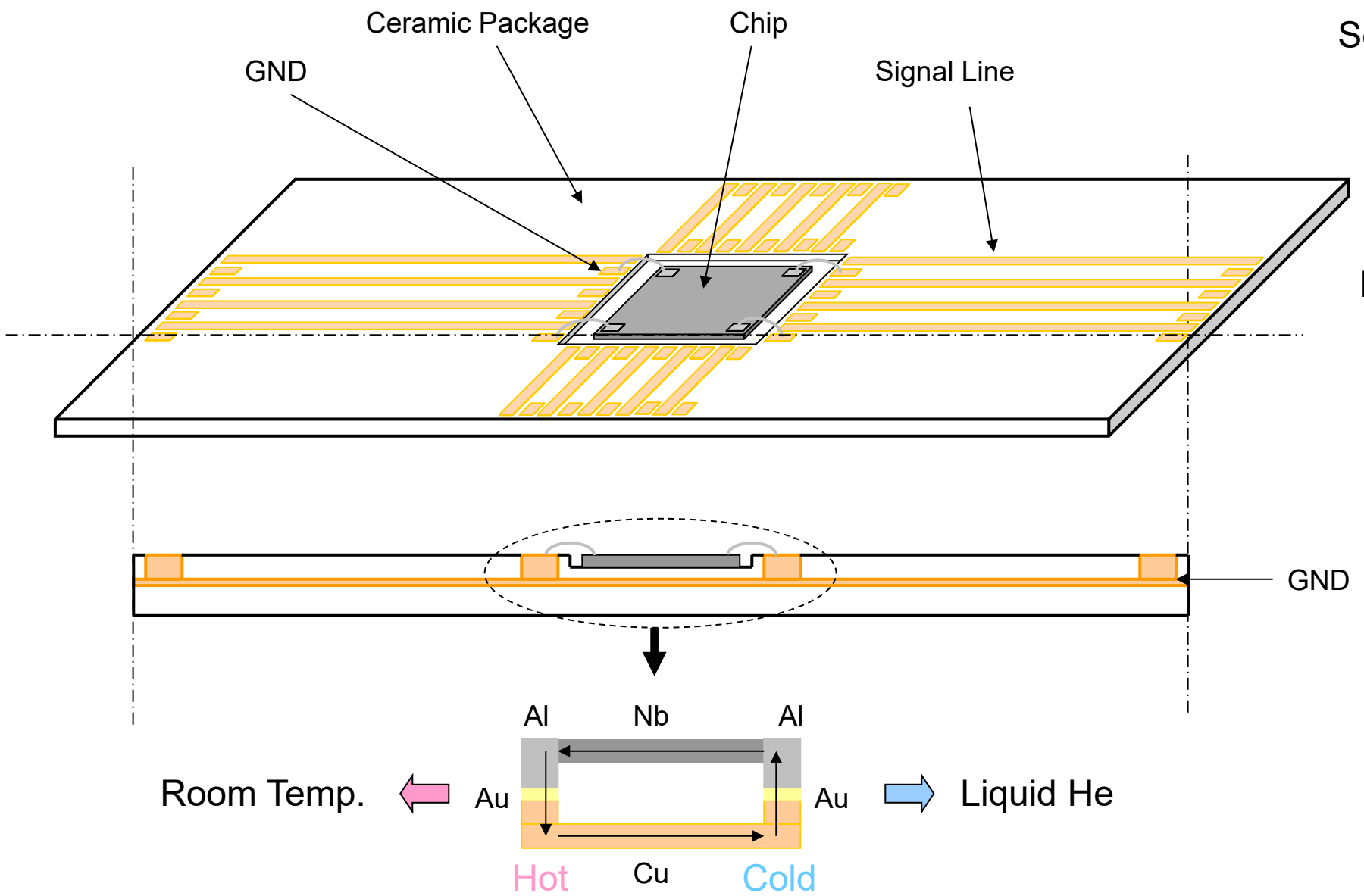
From the trend of magnetic filed reduction, the magnetic field deep inside the shield seems to be in the range of 0.01~0.1 mG.

10 ~ 100 Φ_0 for 5 mm x 5 mm chip

Possible sources of flux trapping

- ✓ **Residual magnetic field due to insufficient magnetic shield**
  - → Triple μ-metal shields may reduce residual magnetic flux below Φ_0.
- ✓ **Magnetization of μ-metal shield**
  - → Requires demagnetization by thermal annealing
- ✓ **Magnetization of screws and other parts around the chip**
  - → Requires frequent check by Gaussmeter and AC demagnetization
- ✓ **Thermoelectric current due to Seebeck effect**
- ✓ **External noise**

Thermoelectric current around the chip



Seebeck effect

ΔT = 1 K → ΔV= 2~3 μV

$R_{Nb} = \rho_{Nb}/300$ nm

= 66 mΩ for ρ_{Nb}=2 μΩcm

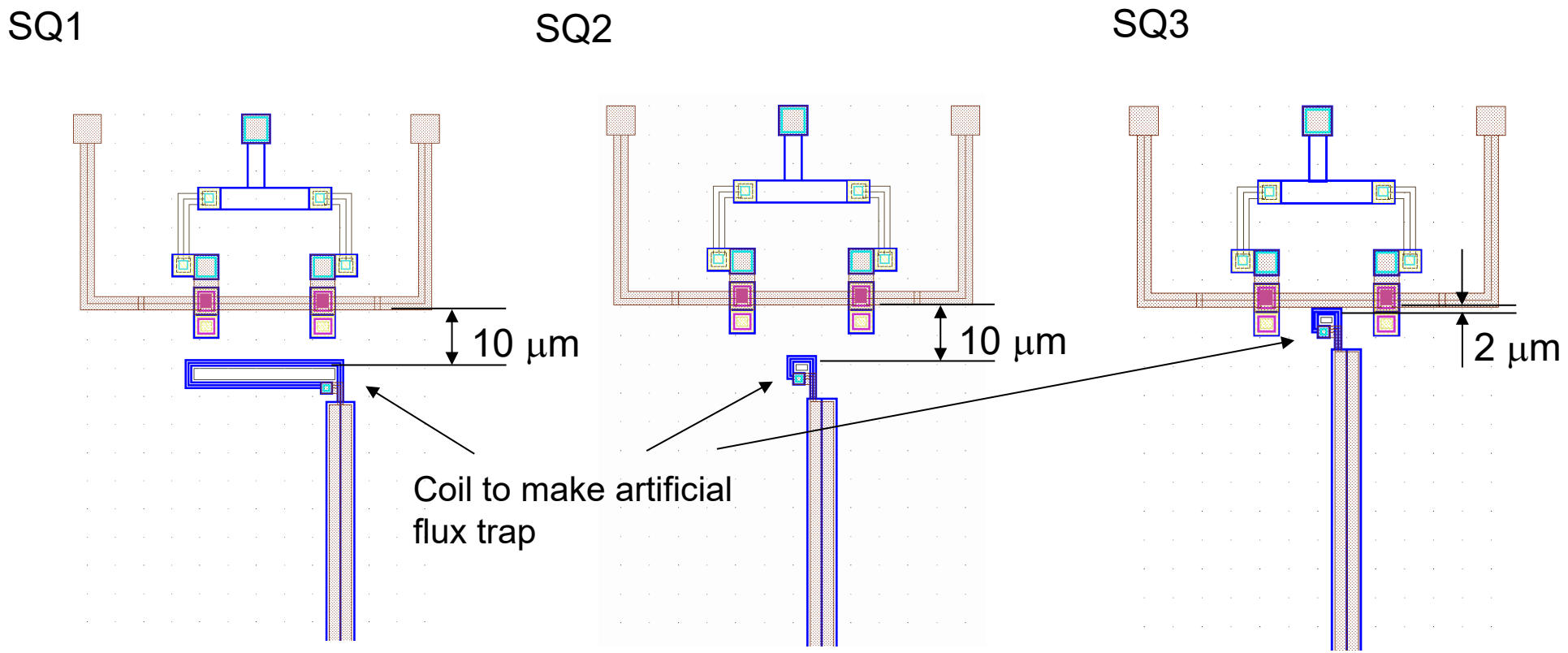
R_{Al}= 20 mΩ/wire

R_{cu} → Negligibly small

R_{loop}~100 mΩ

Thermoelectric current of 2~3 μA for ΔT = 0.1 K

Effect of the artificial flux trap to the SQUID modulation



Moat Area: 2 μm x 25 μm

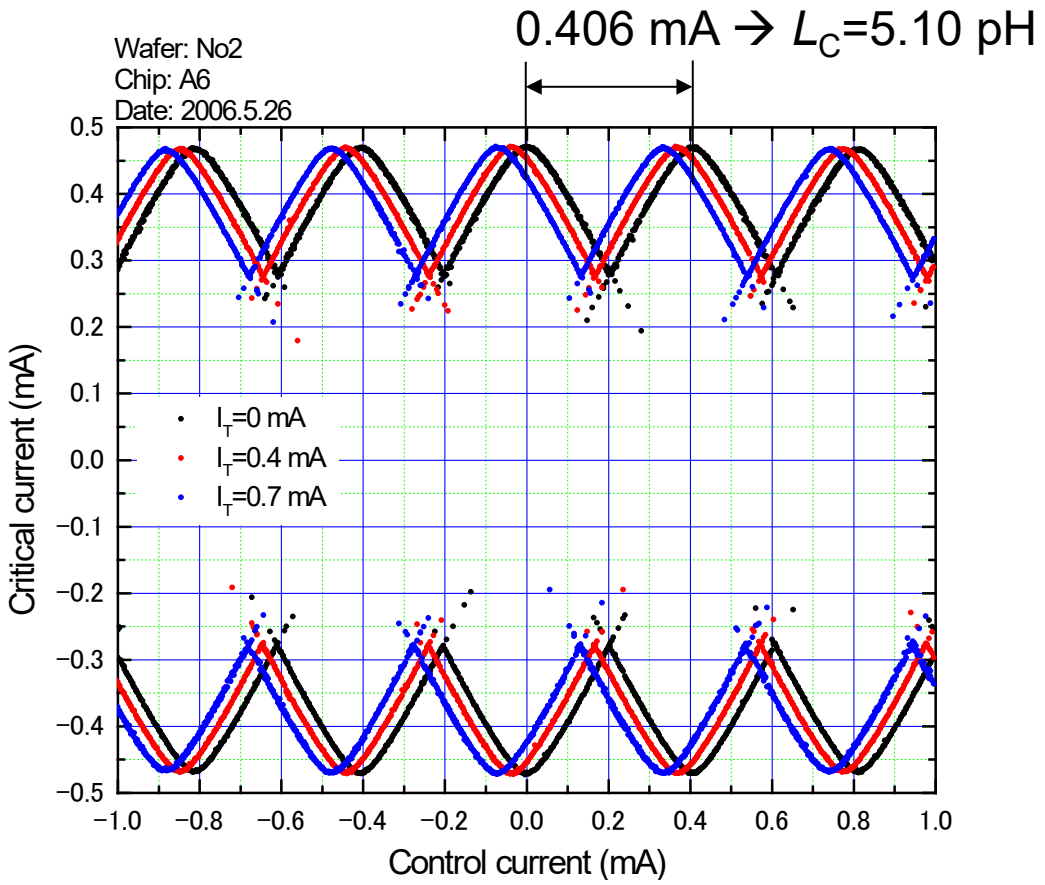
L=35 pH → $I_{\Phi 0}$=58 μA

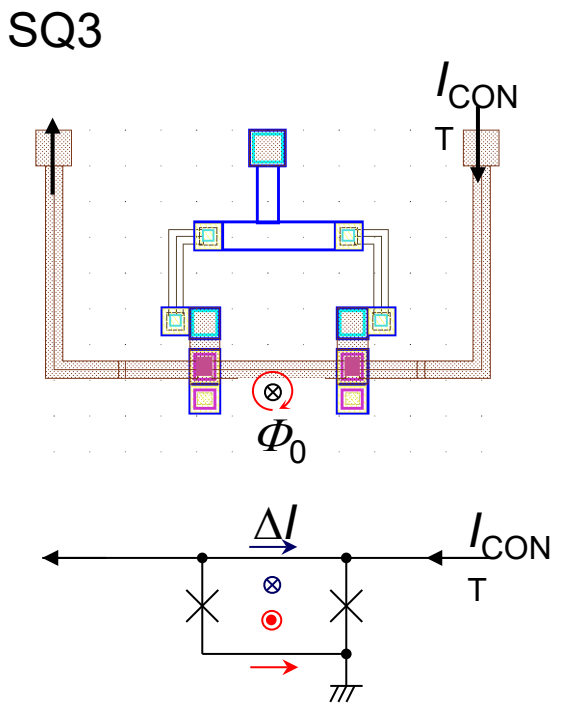
Moat Area: 1 μm x 2 μm

Moat Area: 1 μm x 2 μm

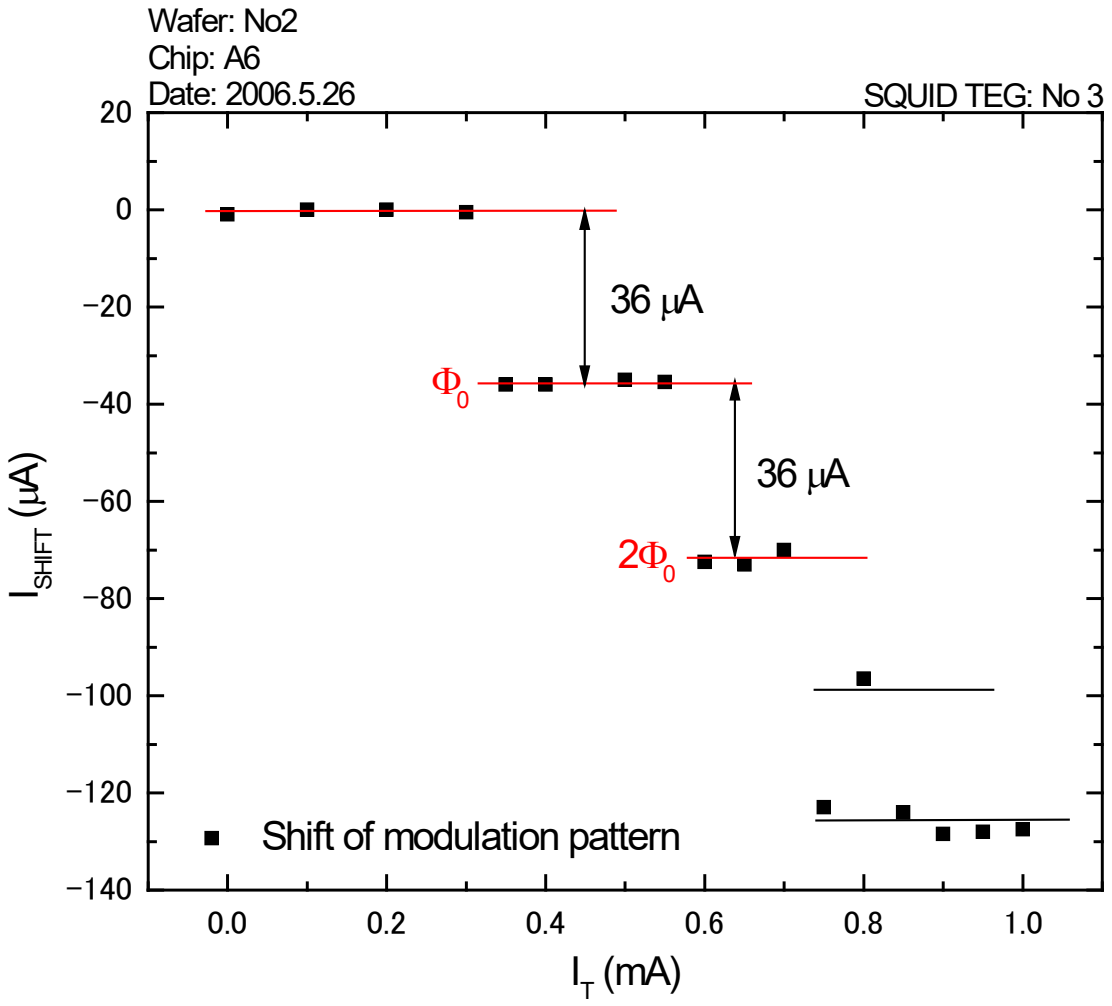
Loop inductance of the SQUID was set to a value close to that of the JTL

SQUID modulation for various coil current





Coil current vs shift of the modulation curve



Shift of modulation curve is quantized by 36 μA

Clear evidence that flux is trapped in the moat

Modulation period is 406 μA

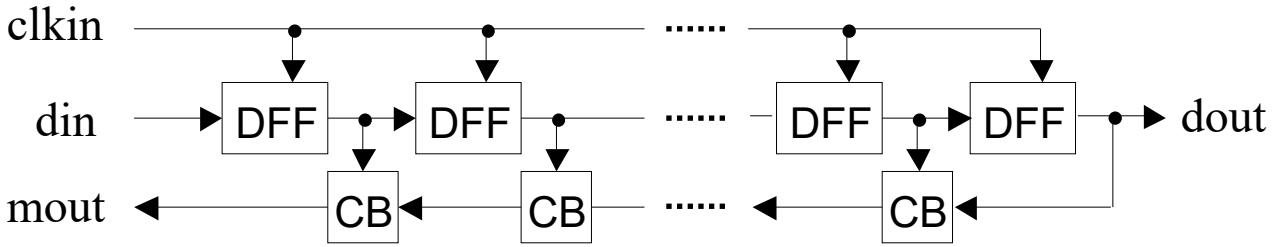
→ 36 μA/406 μA=0.09

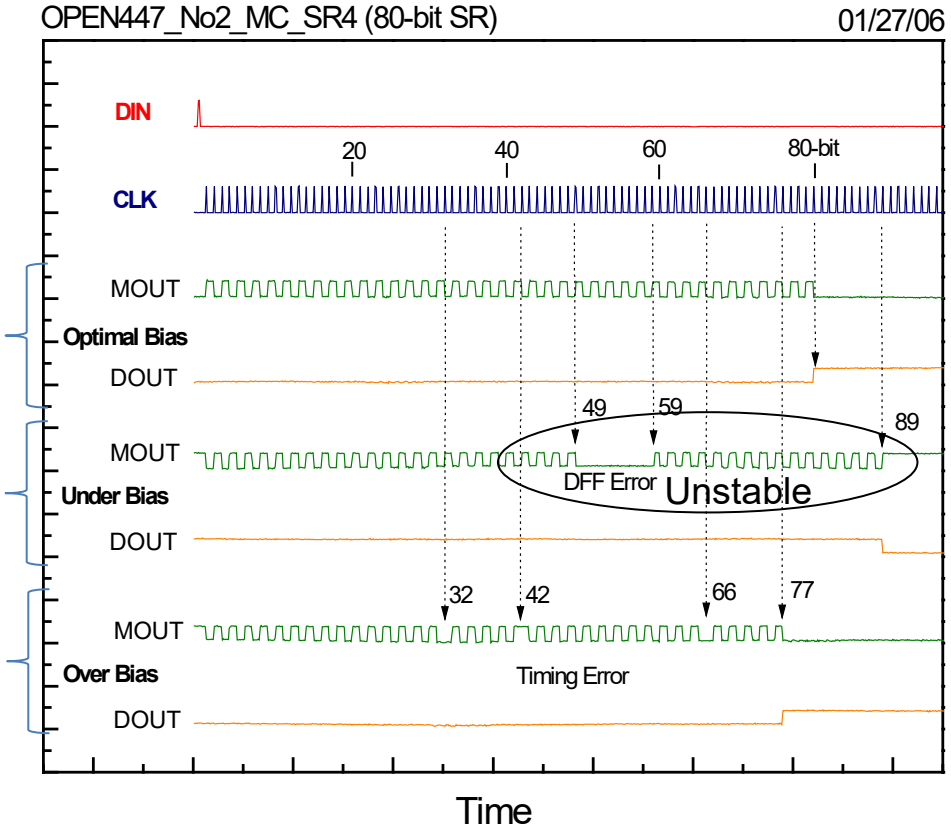
I_C is 455 μA at I_{CONT}=0 for single flux trap,

455 μA/470 μA(I_{CMAX})=0.968

→ 3.2% reduction of I_C

Diagnostic of SFQ shift resister





Step1：Measure bias margin

↓

Step2： Identify the location and type of error from the operating waveforms at the upper and lower margins

↓

Trend of the circuit behavior

Lower margin：Clocking error at DFF is dominant.

Timing errors occur due to flux trap and the effect of bias current

Upper margin：Timing error is dominant.

Output waveform is stable.

↓

Step3：Repeat step1 and 2 after deflux

↓

Identify the cause of the errors (especially whether or not there is a trap)

↓

Step4：Measure other chips

↓

Check reproducibility of errors

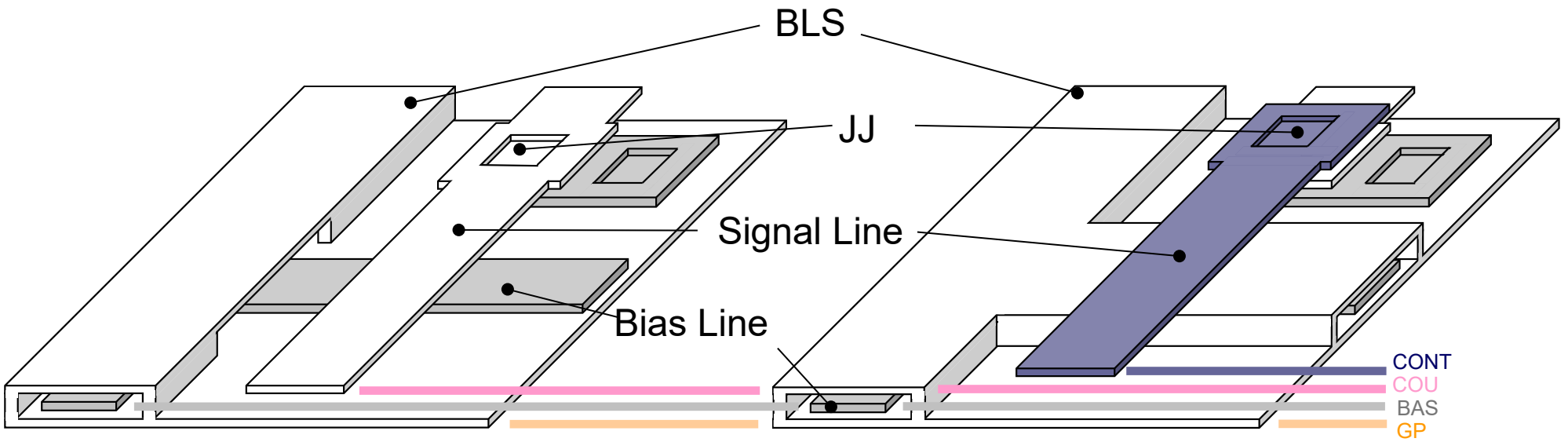
↓

Step5：Measured once again the measured chip if necessary

Bias current shielding in CONNECT cell library

Unshielded bias bridge

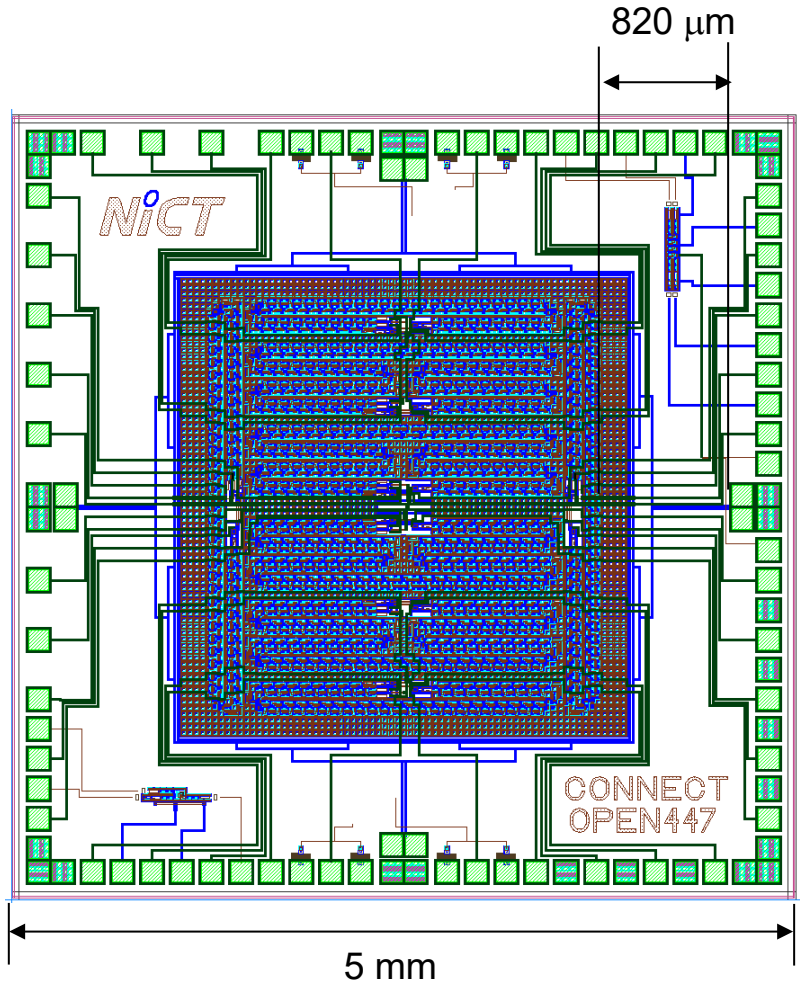
Perfect bias line shield



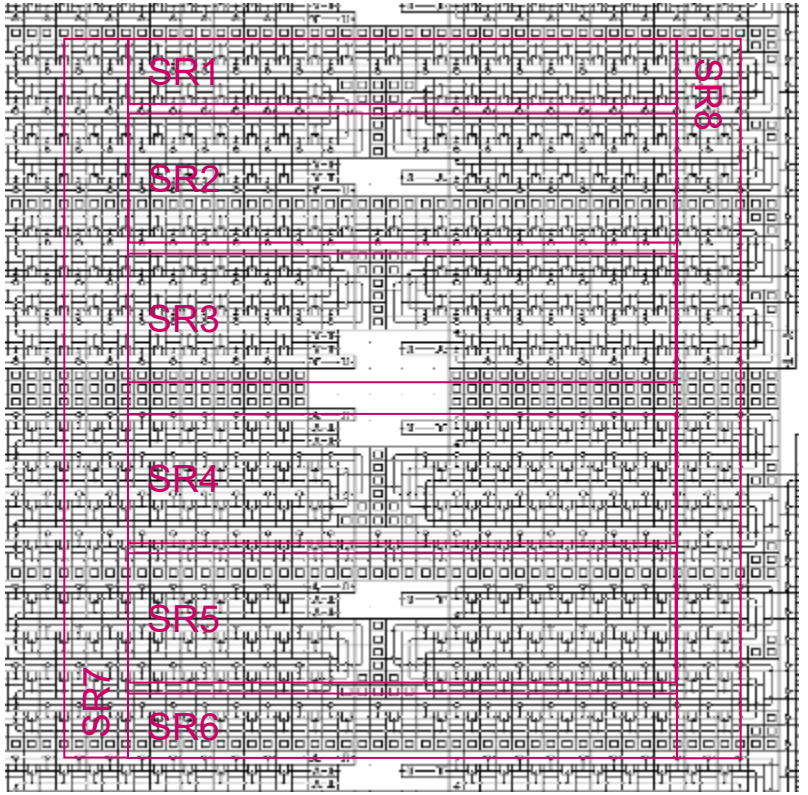
OPEN cell

SUSHI cell
***SU**perconducting **SHI**eld*

Layout of measured chip



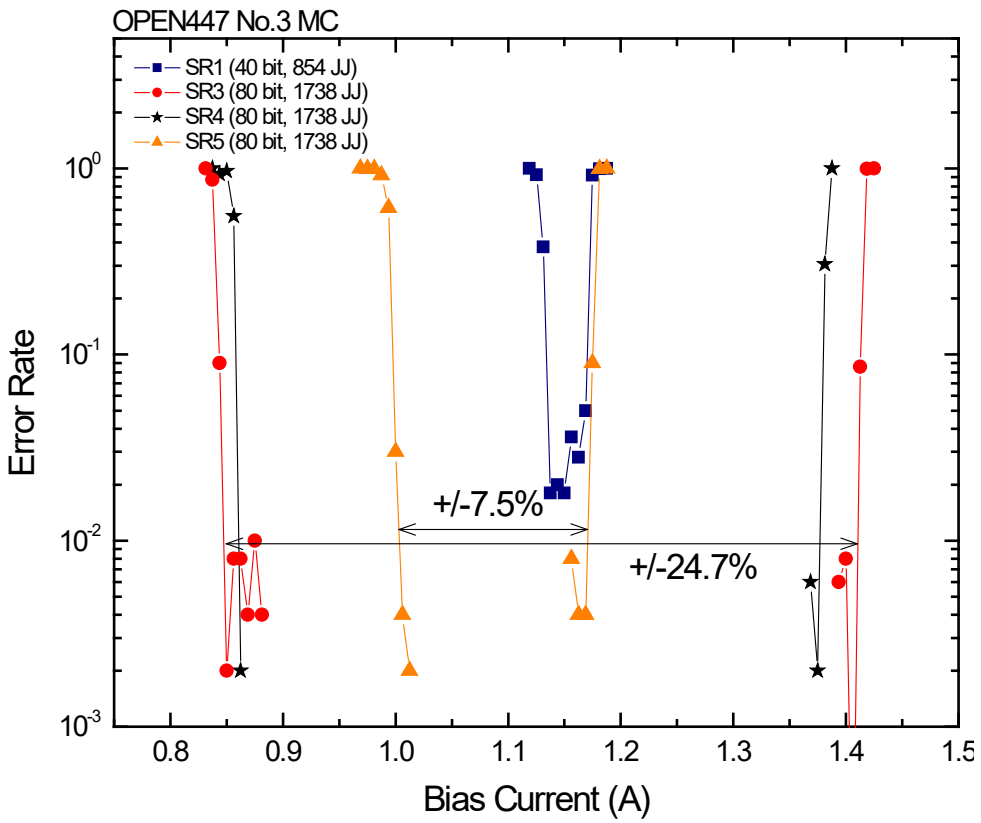
Cell: 2352, **JJ: 10968**, BC: 1.27 A
SR1: 40 bit, SR2: 80 bit, SR3: 80 bit, SR4: 80 bit
SR5: 80 bit, SR6: 40 bit, SR7: 55 bit, SR8: 55 bit



- The circuit is composed of 8 independent DSRs.
- Bias current is supplied through the common bias line.

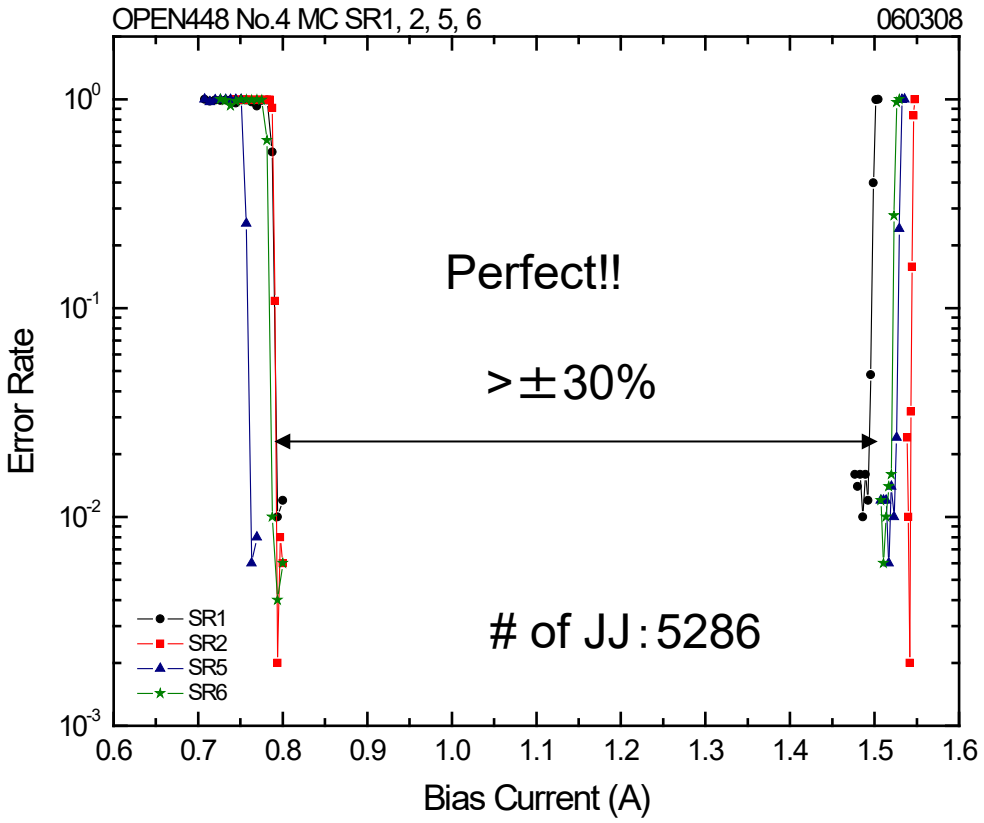
Measured results

Open cell



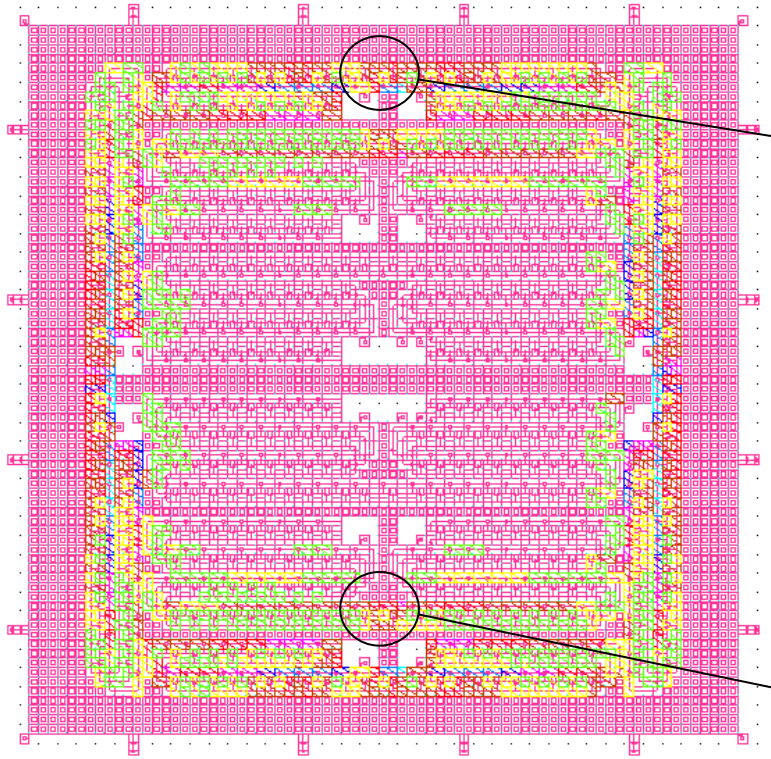
Narrow margin for SR1 and SR5

SUSHI cell



Bias current concentration causes malfunctions in OPEN cells

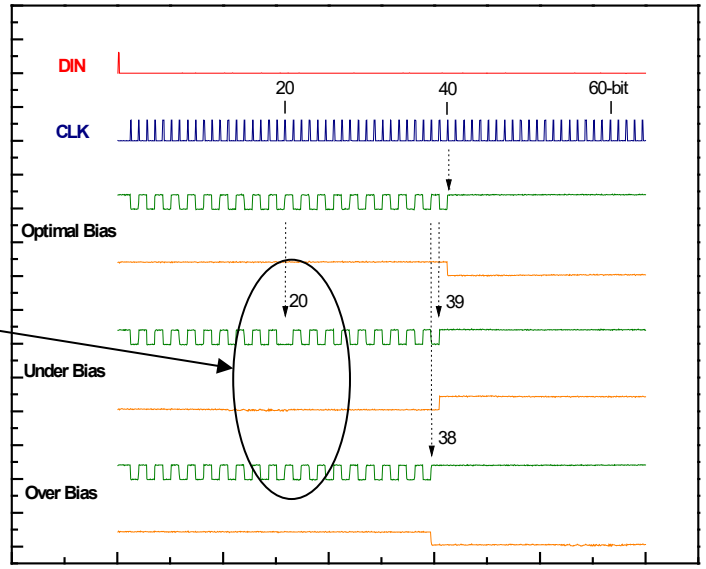
Bias current distribution



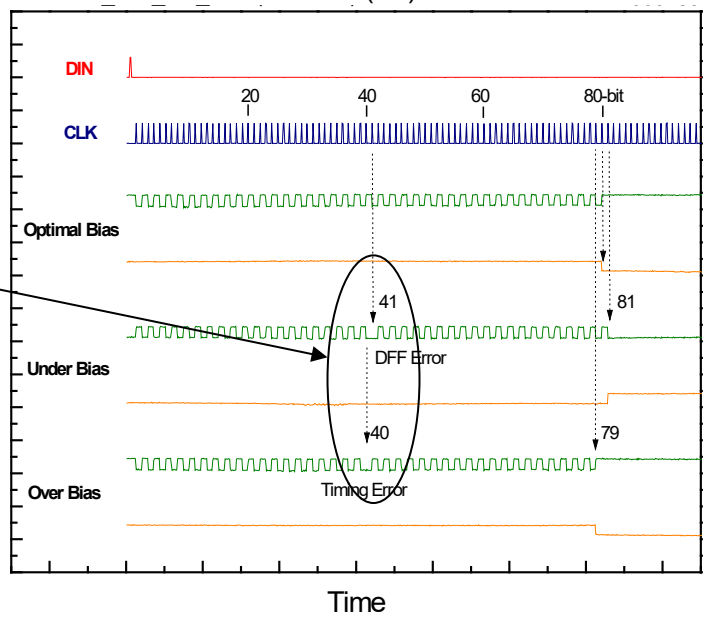
: 10.0mA --
: 9.0mA -- 10.0mA
: 8.0mA -- 9.0mA
: 7.0mA -- 8.0mA
: 6.0mA -- 7.0mA
: 5.0mA -- 6.0mA
: 4.0mA -- 5.0mA
: 3.0mA -- 4.0mA

Maximum bias current
SR1(SR6): ～7 mA
SR2(SR5): ～5 mA
SR3(SR4): ～3 mA

SR1



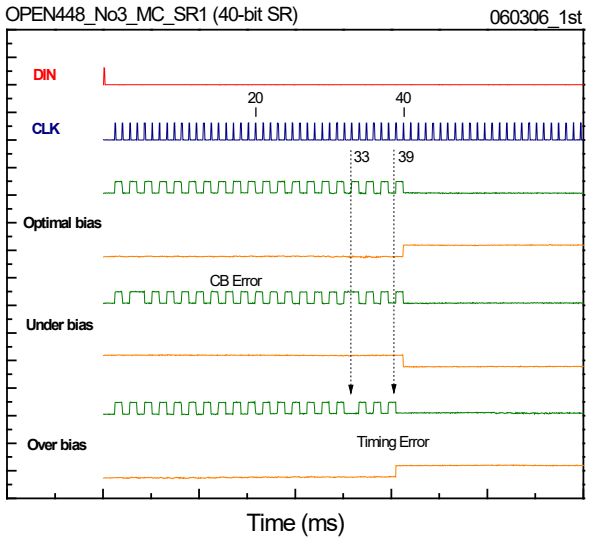
SR5



Effect of trapped flux

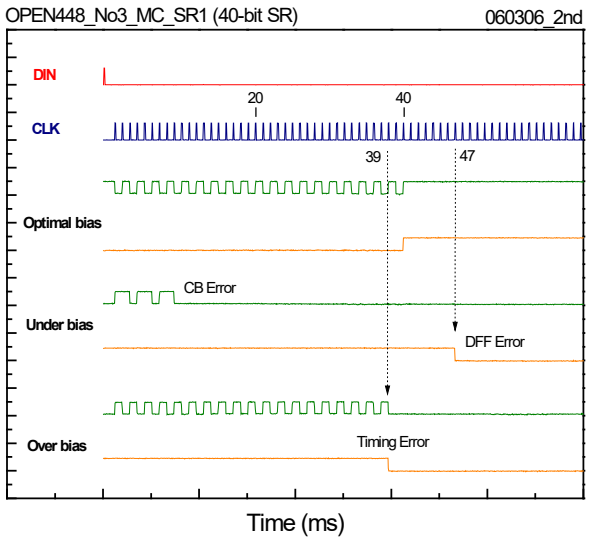
OPEN448 No3 Center chip SR1 with SUSHI cells

1st measurement as cooled



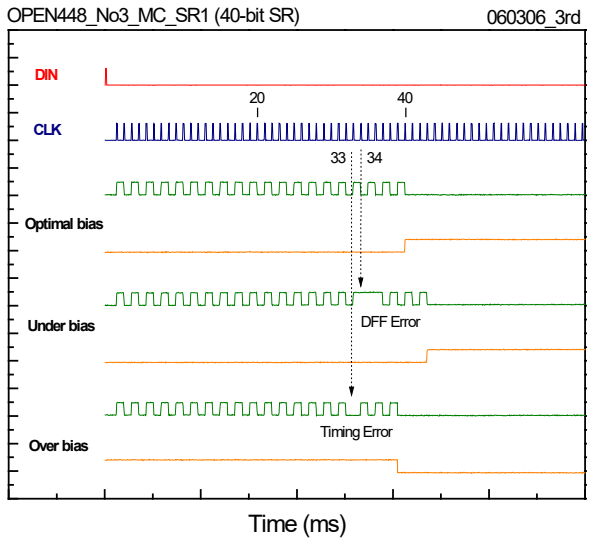
0.911~1.046 A (±6.9%)

After 1st deflux



0.763~1.4 A (±29.4%)

After 2nd deflux



0.905~1.046 A (±7.3%)

In the 1st and 3rd measurement, bias margins were narrow due to the errors at 33rd bit

→ Flux is trapped at the same position!

Summary

- ✓ We introduced our recent activities on cryogenic signal processing for SNSPD array to enhance the performance of SNSPD.
  - Dc current supply to SFQ circuits is a key issue to realize the large-format SNSPD array.
  - Dc current supply of ~1 A will be possible by employing non-magnetic μ-Dsub connectors.
- ✓ We introduced our old activities on circuit diagnostic to reveal the origin of circuit errors.
  - The origin of flux trap remains unclear despite significant efforts to reveal it.
  - Trapped flux at the moat may affect the circuit operation when the moat is too close to the circuit.
  - The position of flux trap is sometimes reproducible.

    → Non-uniformity of superconducting properties of GP may cause flux trap.
    We are trying to test epitaxial NbN films as GP in the future.
  - More general diagnostic method for large-scale SFQ circuit will be required.

Diagnostic of SFQ circuit using DSR

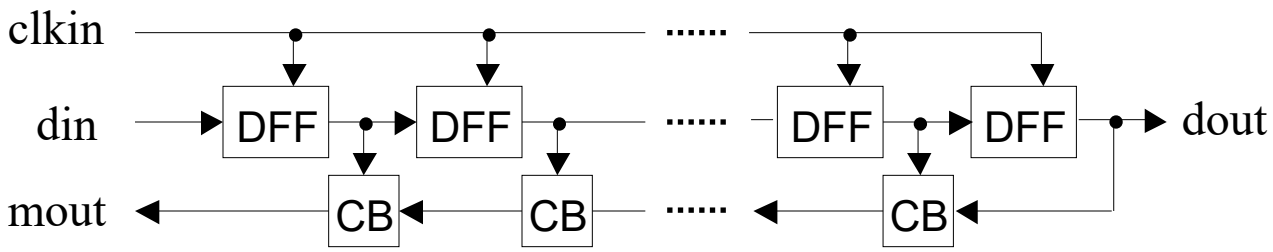


Fig. Block diagram of diagnostic shift register (DSR)

Optimal bias

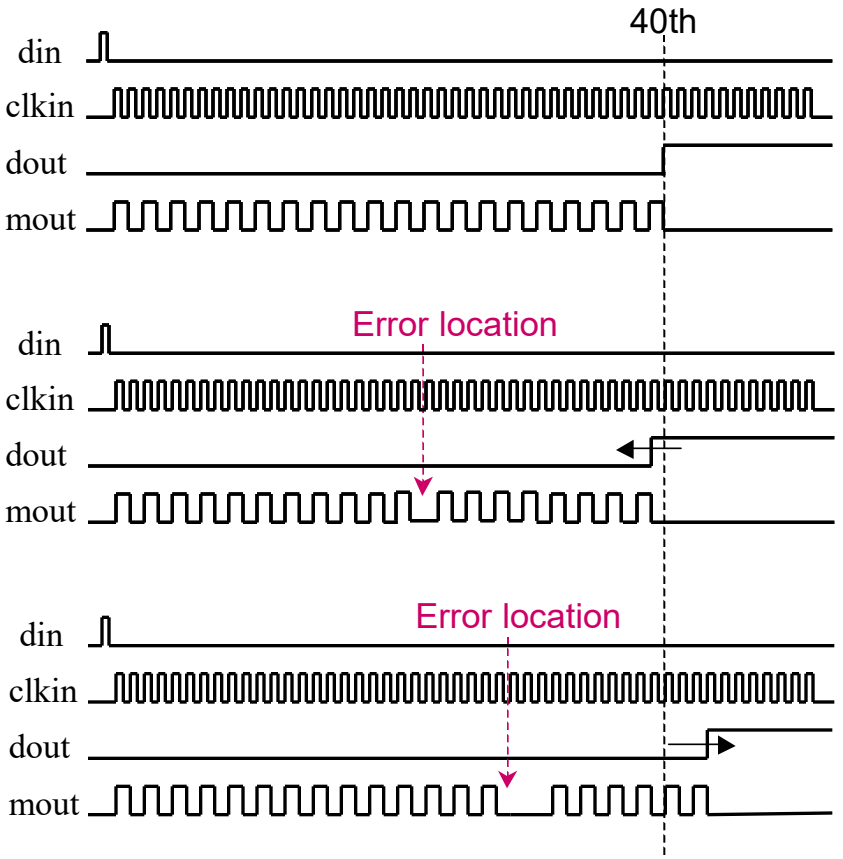
The number of pulses appeared at output “mout” corresponds with the number of DFFs.

Over bias

Timing error occurs at a location with the lowest margin. We can identify the error location.

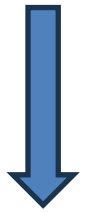
Under bias

If flux trapping exists, timing errors occur before this waveform appears.



Residual magnetic flux on 5 mm x 5 mm chip

Earth magnetic field: 300~500 mG



1-mm-thick μ-metal shield → -20 dB

Magnetic field inside the dual μ-metal shield: 0.03~0.05 mG

→ Comparable to the measured magnetic field of 0.01~0.1 mG

5 mm x 5 mm chip:

0.1 mG → $\Phi = 10^{-8} \times 25 \times 10^{-6} = 250 \times 10^{-15}$ Wb = 121 Φ_0

0.03 mG → **36 Φ_0** for 5 mm x 5 mm chip

Triple μ-metal shied may reduce residual magnetic flux below 1 Φ_0.