SYNOPSYS®

Toward Trapped Flux Insensitive SFQ Logic Circuits

Potential Magnetic Mitigation Strategy

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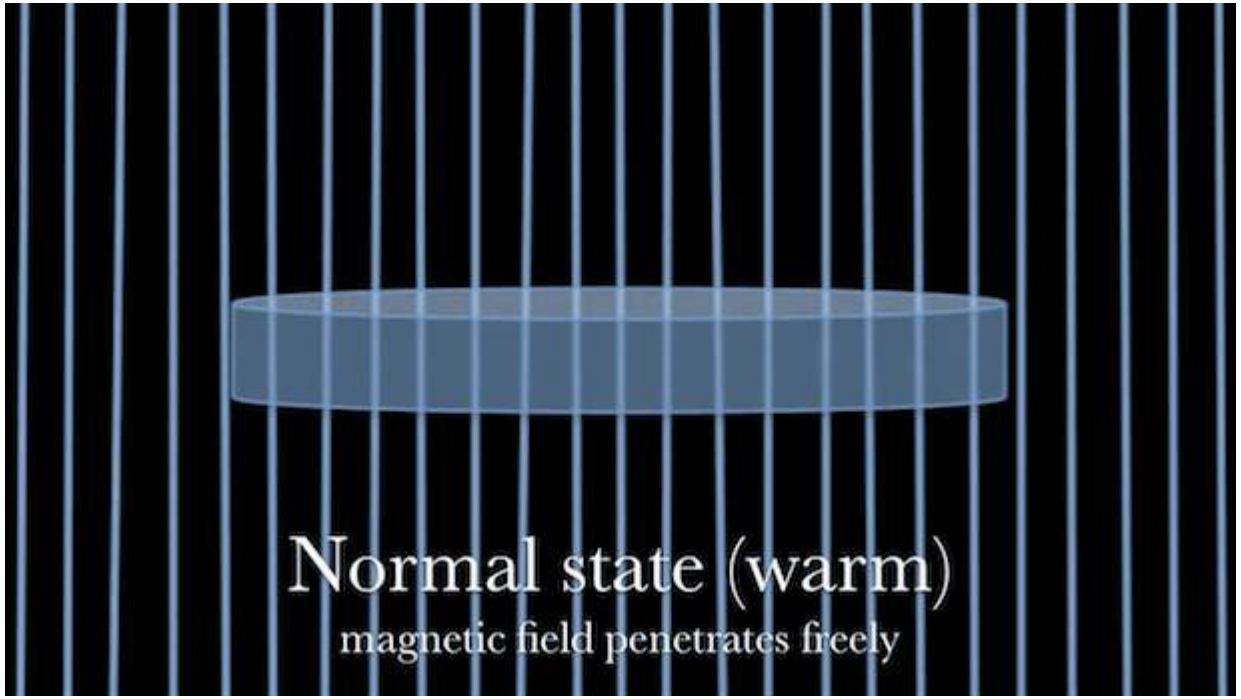
What is Trapped Flux?

- Magnetic flux can easily penetrate normal metals, including superconductors above Tc.
- When a superconducting film cools down from above to below Tc in the presence of a magnetic field:
  - Cooling isn’t perfectly uniform and islands of superconducting and normal regions transiently exist.
  - Energetically, magnetic lines of flux are pushed into the normal areas, or expelled at edges of the film where superconducting.
  - Flux that remains when the normal regions become superconducting becomes trapped.
  - The trapped flux creates a circulating current in the superconductor around a hole or tiny core forced normal. The flux will find existing holes or defects where it becomes trapped.
  - This structure has an integral number of flux quanta due to continuity of the wave function.
  - The associated magnetic field can cause bias shifts in nearby Josephson circuits.

Flux Trapping Cartoon

http://ffden-2.phys.uaf.edu/webproj/212_spring_2017/Nick_Brazier/nick_brazier2/Superconduction_Basics.html



Avoiding Trapped Flux: Standard Tricks

Two sources for trapped flux:

1. Flux trapped during cool-down as described previously.
2. Flux trapped during catastrophic overload event:
   - Exceeding the critical current of circuit wires, due to static discharge or simple overdrive. Use a wrist ground strap when testing. Do not connect coaxial cables that are not connected to something else that will discharge them. Etc, use common sense.
   - Too much heat generated by a resistor or some other heat source on-chip.

Use magnetic shielding (both are expensive but necessary):

1. External (room temperature) mu-metal shield.
2. Internal (4K) cryo-perm shield.

Well designed chip fixturing:

1. Scrupulously avoid magnetic bits and pieces (screws and hardware, wire, pogo-pins).
2. Chip orientation such that chip normal is horizontal (my personal experience).
3. Have a defluxing coil and use it periodically (and use it properly!).

Avoiding Trapped Flux: Some Mitigations

Arrange cooling so that transition front is linear and sweeps across chips. This will tend to sweep flux off the edge of the chip rather than it being caught in islands of normal area.

Cool slowly, again to avoid transient normal islands where flux is trapped. When inserting into a dewer, pre-cool in gas for a few minutes before slowly immersing.

Some fixturing has “defluxing” heaters. These may or may not work well in practise, but the concept should be good. Something like this would probably be required in “real” systems.

Avoiding Trapped Flux: More Mitigations

There is much lore about layout strategy to avoid trapped flux.

1. Avoid large expanses of ground plane.
2. Use “moats” (holes in the ground plane) to provide safe trapping locations away from devices. Larger area is better (probably). Many designers and facilities have their own guidelines about moat placement.
3. Normal metals such as aluminum or gold may be useful to supplement ground plane to avoid large superconducting loops.

Trapped flux is statistical. There is no way to guarantee that no flux is trapped, but probability of trapping can be made low.

Can we design circuits that are insensitive to trapped flux?

Magnetic Interaction in Superconductor Circuits

As we go to higher critical current density, individual Josephson junction sensitivity becomes less, as junction lateral size decreases. Higher critical current density is better for reduced sensitivity to stray fields.

All known Josephson junction circuits contain geometric loops including Josephson junctions. These loops are “SQUIDS” and are sensitive to magnetic fields, including from trapped flux. This sensitivity dominates the junction sensitivity in current logic circuits.

If we could build logic gates/flops without superconducting loops, then these circuits would be substantially insensitive to trapped flux (and other static magnetic fields, such as the Earth’s). Put on your thinking caps!

The next best thing would be to use kinetic inductance in these loops instead of geometric inductance. Unlike geometric inductance, kinetic inductance does not couple to magnetic fields. However, some small geometric inductance would remain, so residual sensitivity would remain. This only applies to technologies that don’t need transformers, e.g. SFQ but not AQFP.

Introducing YSFQ, Synopsys Prototype Next-Gen SFQ Process

- Baseline is Lincoln Laboratory SFQ5ee process, but with 0.6mA/μm^2 self-shunted Josephson junctions.
- Uses series arrays of Josephson junctions instead of inductors ($L_J = \Phi_0/(2\pi I_c \cos(\varphi))$). The only inductance found is parasitic, or possibly part of a transformer in future cells. This provides the following advantages:
  - Tracking of I_cL product with J_c global variation for increased circuit yield.
  - Reduced sensitivity to magnetic fields for lower crosstalk and lower sensitivity to power currents and trapped flux.
  - Reduced circuit area and greater flexibility of feature placement in layout, scalability.
- Uses voltage-biased (no feeding JTL) ERSFQ biasing at all bias points, keeping the bias circuitry as logical components of the library cells. This provides bias tracking of J_c global variation for high circuit yield.
- Uses high impedance (16 ohm) PTL interconnect for lower current operation.
- Integrated PTL driver/receivers, no additional circuitry when possible.
- Uses wired-OR capability for cost-free OR logic.

YSFQ New Features

- Circuits consist entirely of Josephson junctions, plus discrete resistors and PTLs for interconnect, and high-inductance kinetic inductors as filters in the ERSFQ biasing networks.
- Thus all circuits are largely insensitive to global critical current density changes, though there is a “sweet spot” defined by chosen transmission line impedance, and higher critical current density (really CPIC) should provide higher-speed operation. JJ area ratios define everything.
- The tracking of bias currents and critical current density enables higher sensitivity at PTL inputs, enabling the wired-OR capability. One can define operating points closer to the critical currents of junctions, for shortest delays, due to the tracking.
- Complementary Asynchronous (Synopsys patented asynchronous logic) implementations for UAND, XOR.
- Overall advantages over existing libraries:

  1. Higher density, 2. Low Magnetic Sensitivity and Scalability (no inductors), 3. Lower Power (lower Ic from higher PTL Z).

YSFQ Next Generation SFQ Fabrication Process

We take as a baseline the Lincoln Laboratory SFQ5ee process with the following improvements:

1. Use of **self-shunted 0.6 mA/μm² Josephson junctions**, as developed (but not productized) at Lincoln Laboratory.
2. The availability of a **high Jc kinetic inductance layer** material which will not limit layout density.
3. Use of **trench grown transmission line structures** that support submicron routing pitch.

For our simulation work, only #1 is relevant, but 2, 3 are likely required for adequate density in applications.

The Josephson junctions require use of a **tunnel junction model**. See paper from last ASC:

Observations in Use of a Tunnel Junction Model in Simulations of Josephson Digital Circuits,
Stephen Whiteley, Aaron Barker, Eric Mlinar, Jamil Kawa, Sukanya S. Meher, Jushya Ravi, Amol Inamdar,

IEEE Transactions on Applied Superconductivity, vol. 33, issue 5, id. 3232057 August 2023

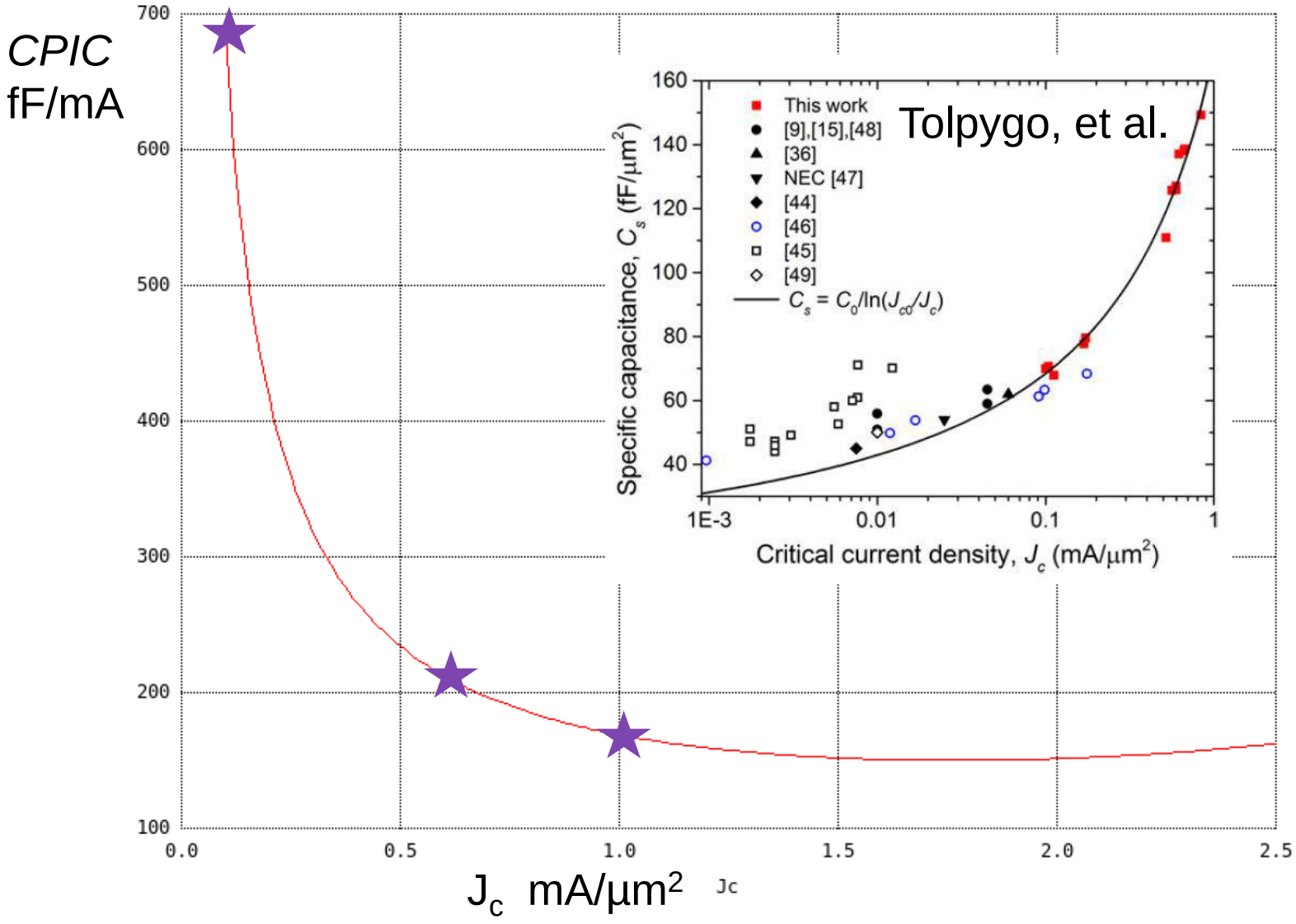
Model is available in Synopsys HSPICE, WRspice.

CPIC Behavior With J_c Variation May Be Surprising

$$CPIC = \frac{C_0/J}{\log(J_{c0}/J)}$$

From Tolpygo: C_0 = 0.265 +/- 0.015 pF/μm², J_{c0} = 4.8 +/- 0.5 mA/μm².

Tolpygo, et al. *IEEE Trans. Appl. Supercond.* vol **27** no 4 1100815 June 2017.



- *CPIC* falls rapidly below 0.5mA/μm² which is good.
- Larger critical currents give diminishing improvement. Pointless to operate above ~1mA/μm² for performance, but JJ areas still shrink.
- Lowest *CPIC* = 0.150 pF/mA at $J_c = J_{c0}/e$ = 1.77 mA/μm²

Our 3 reference points:

Status	J_c mA/μm²	*CPIC* pF/mA
LL SFQ5ee	0.1	0.685
LL LSI demo	0.6	0.212
future	1.0	0.169

Josephson Junction Counts Per Cell

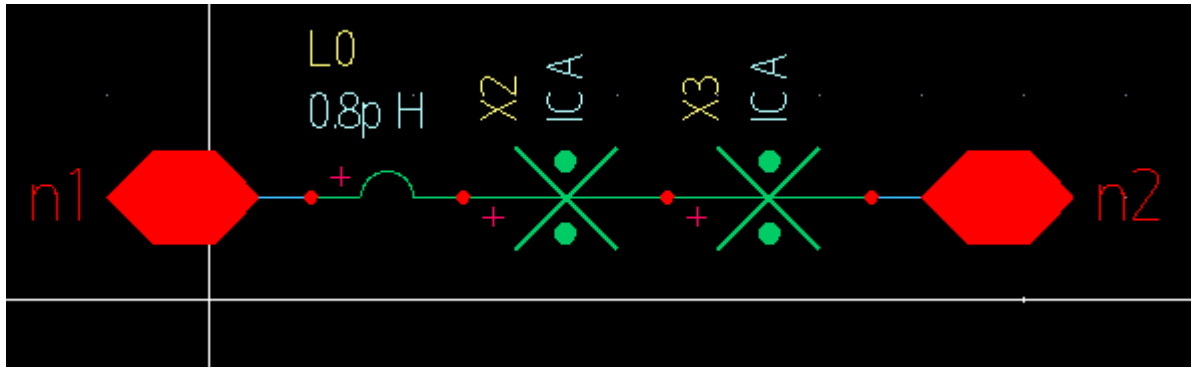
Ind is JJs used as inductors, **Pwr** is JJs used for power points (one per bias tap), **Ckt** is JJs used as circuit JJ elements.

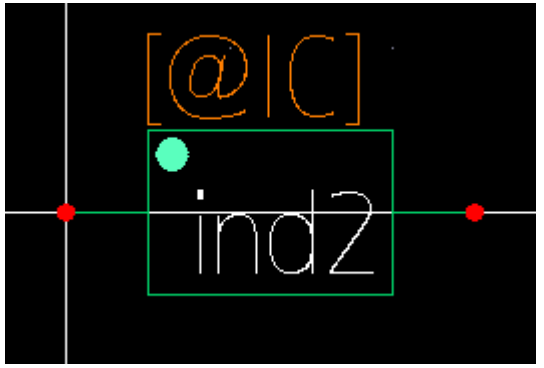
Cell	Total	Ckt	Pwr	Ind
and	39	12	5	22
and2	45	13	6	26
buf	7	2	1	4
buf0	7	2	1	4
buf2	13	3	2	8
bufb	7	2	1	4
cadffx	222	64	30	128
cauand	147	38	17	92
caxor	281	80	37	164
dpbuf	7	2	1	4
dpbuf2	13	3	2	8
dpdrvr	10	2	2	6
ersfq	1	-	1	-
inv	41	11	4	26
inv2	47	12	5	30
jjind2	2	-	-	2
jjind4	4	-	-	4
ndsa2	40	12	6	22
ndsa22	80	24	12	44
ndsal	27	7	4	16
ndsar	27	7	4	16
xor	40	12	6	22
xor2	46	13	7	26

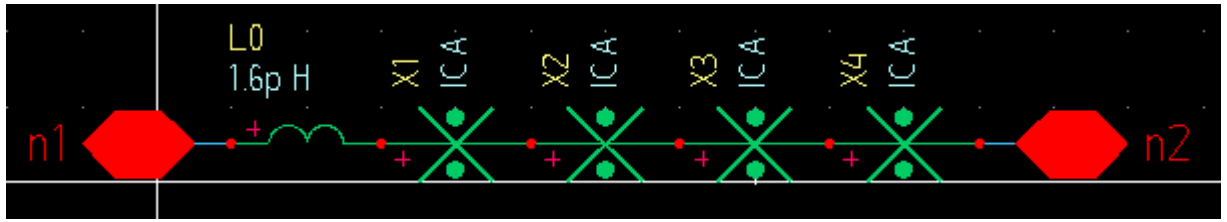
Cell	Total	Ckt	Pwr	Ind
srff_o0	17	4	1	12
srff_o0n2b	57	16	7	34
srff_o0nlb	44	11	5	28
srff_o0nrb	44	11	5	28
srff_o2	17	4	1	12
srff_o2b	31	8	3	20`
srff_o2bn2b	71	20	9	42
srff_o2bnlb	58	15	7	36
srff_o2bnrb	58	15	7	36
srff_o2bn22b	111	32	15	64
srff_ol	17	4	1	12
srff_olb	24	6	2	16
srff_olbn2b	64	18	8	38
srff_olbnlb	51	13	6	32
srff_olbnrb	51	13	6	32
srff_or	17	4	1	12
srff_orb	24	6	2	16
srff_orbn2b	64	18	8	38
srff_orbnlb	51	13	6	32
srff_orbnrb	51	13	6	32

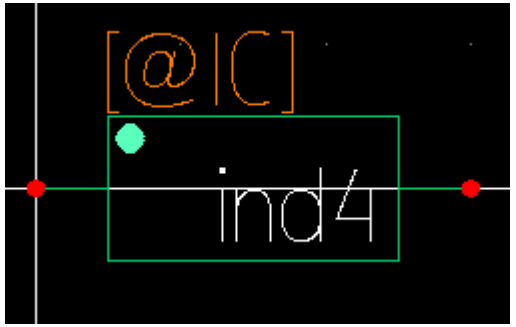
Cells: `jjind2, jjind4`

Description: “inductor” cells, assume 0.4pH parasitic series inductance per JJ.



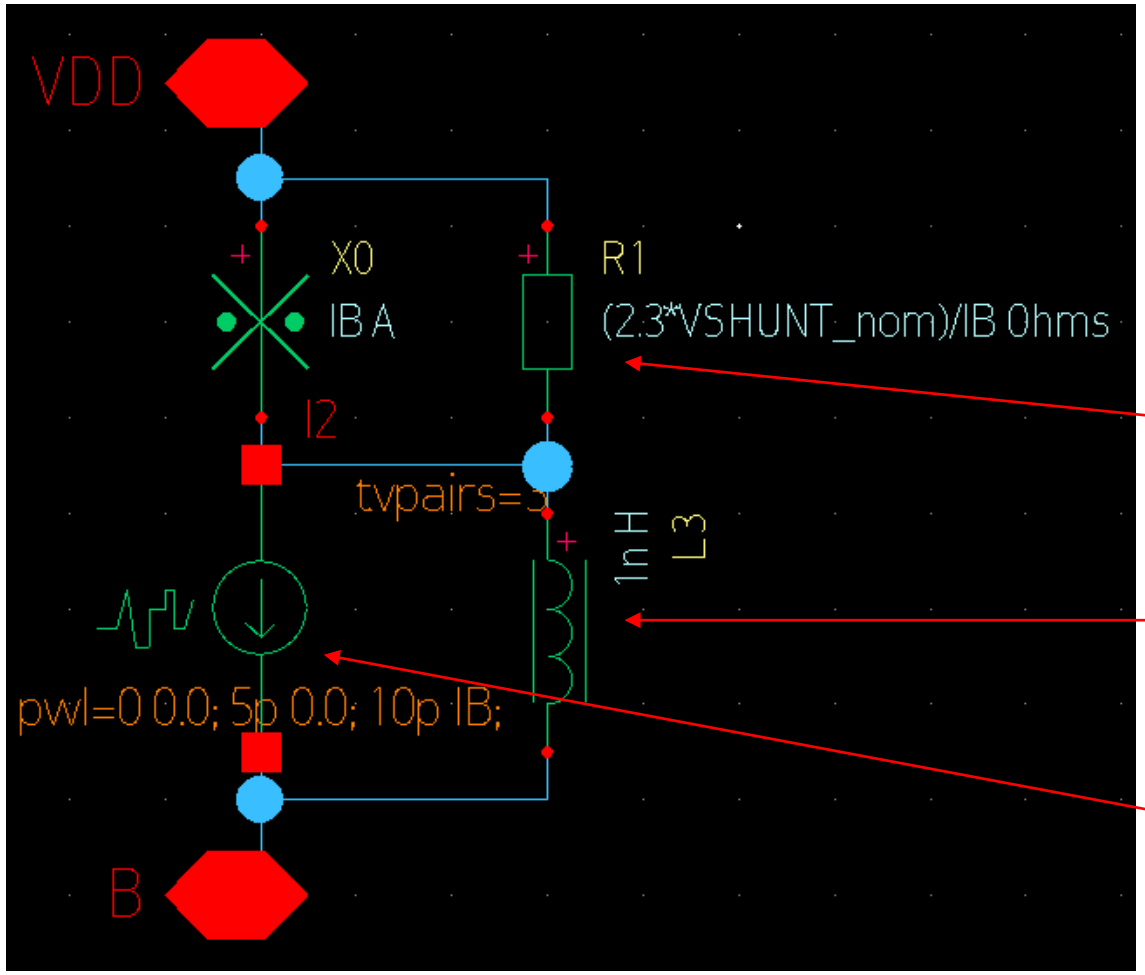


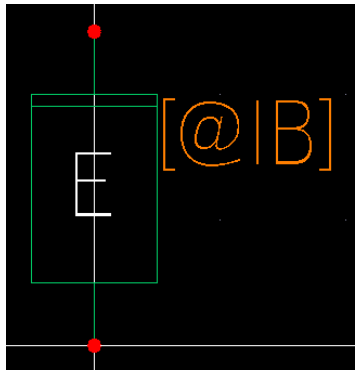




Cell: ersfq

Description: bias current source.





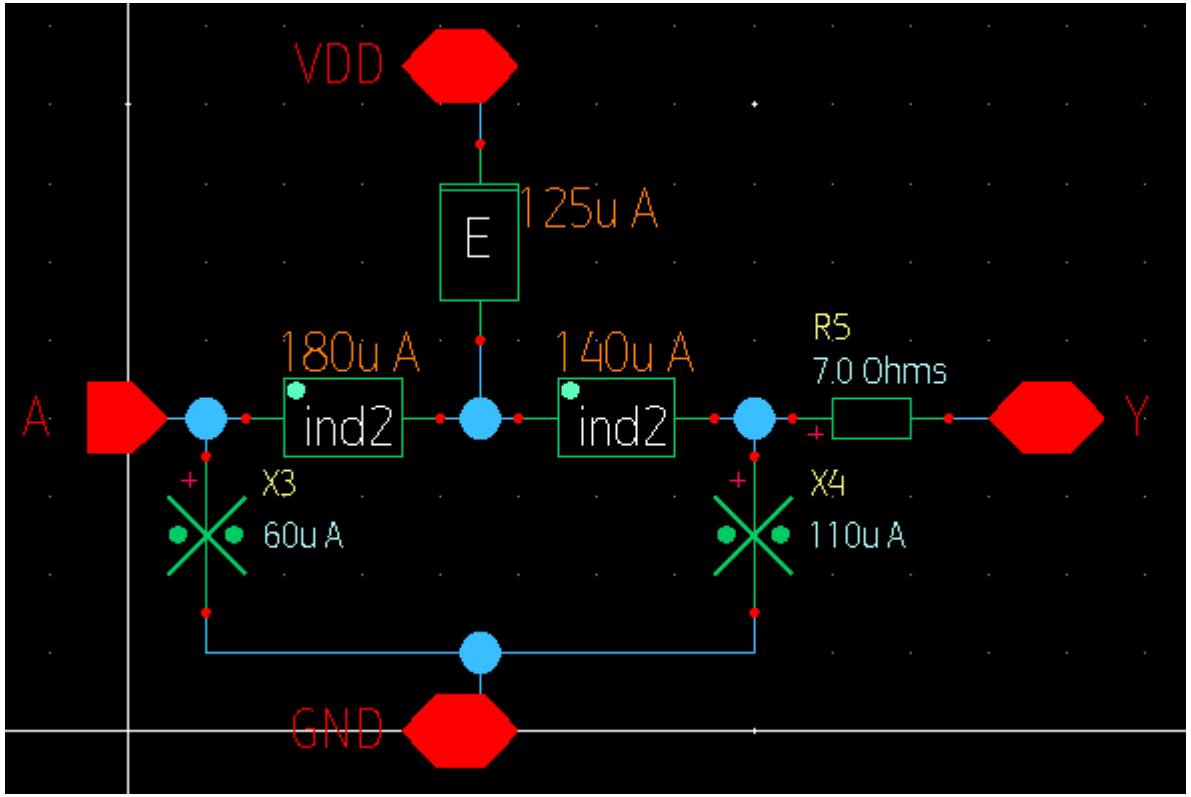
Needs additional damping, extra resistor assumed.

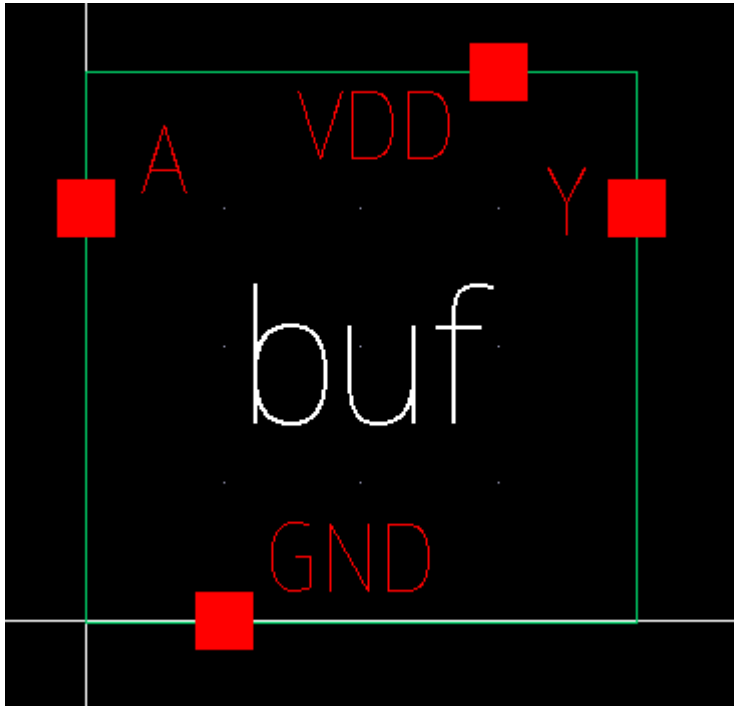
Kinetic inductance filter inductor.

Hack to avoid startup delay in simulations.

Cell: `buf`

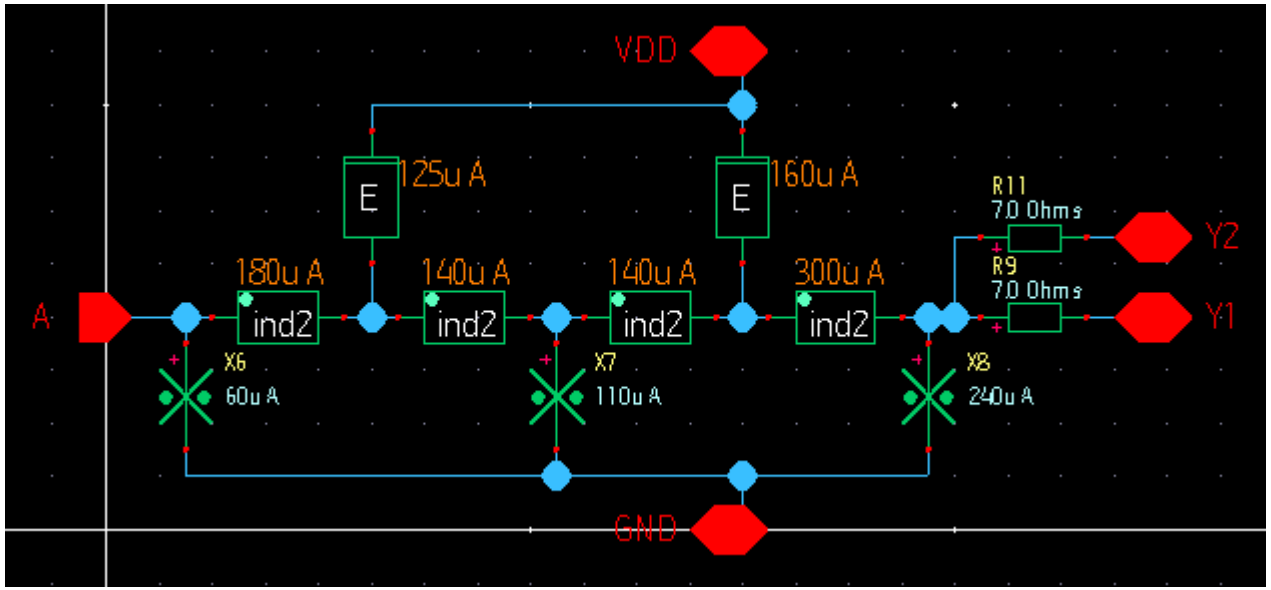
Description: original design non-clocked buffer. Note direct connection to PTLs.

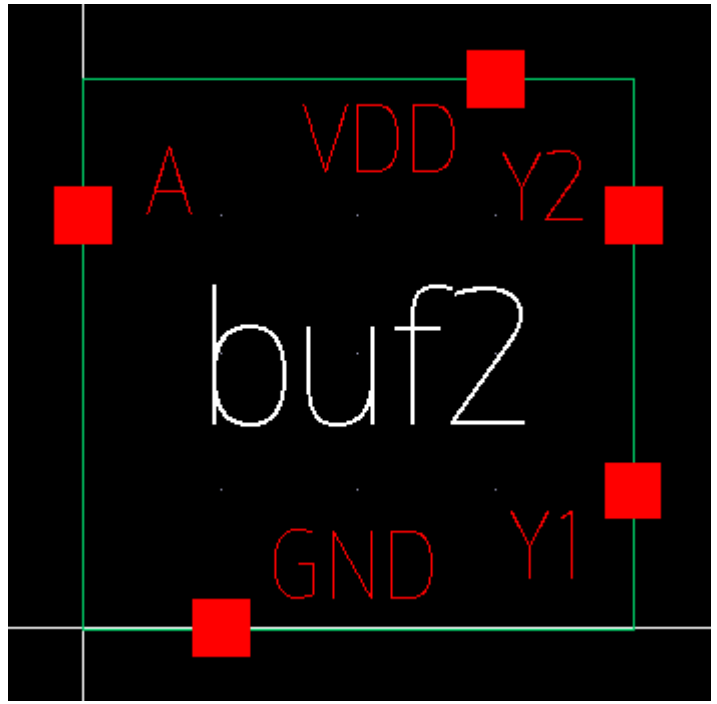




Cell: `buf2`

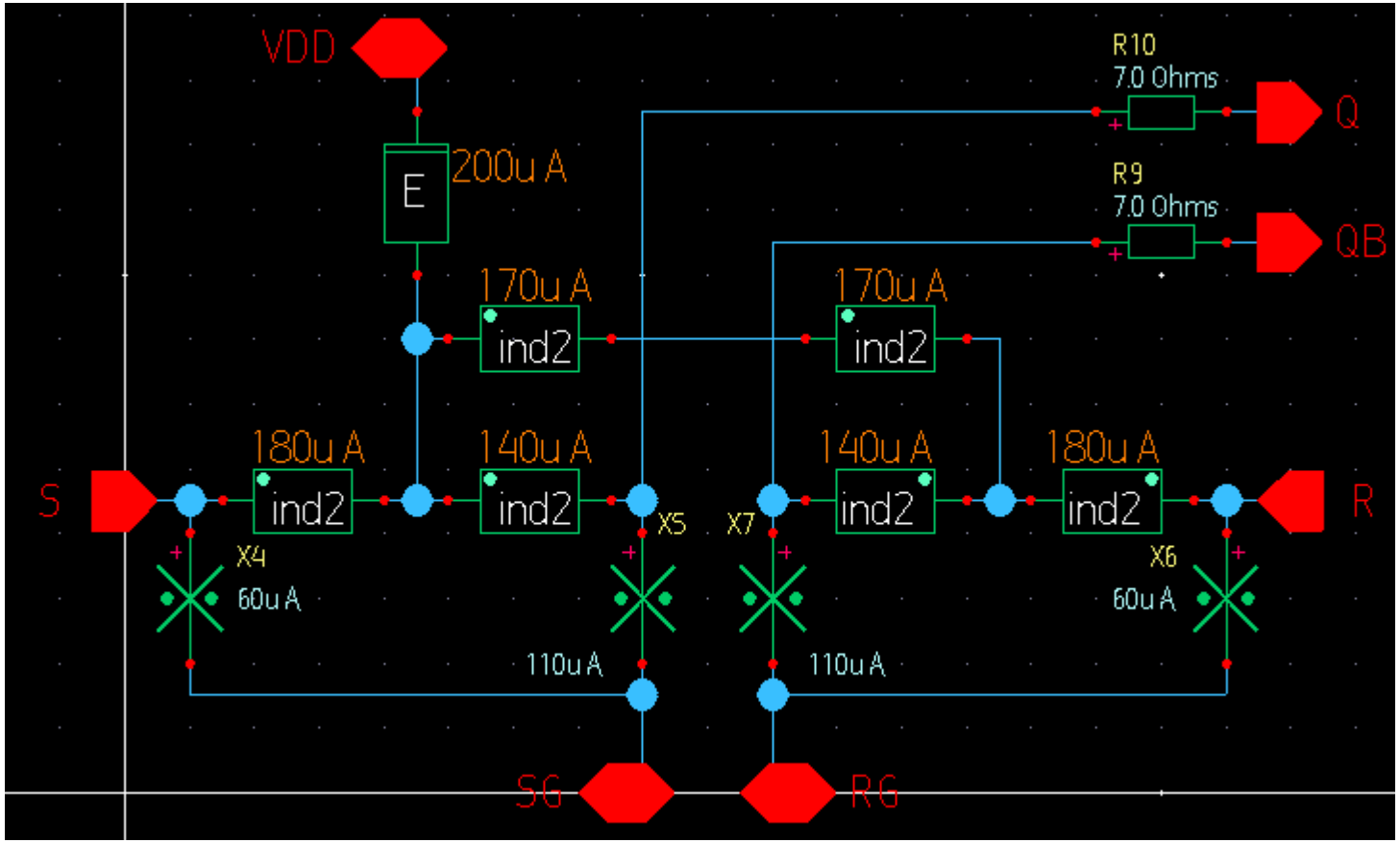
Description: Original design non-clocked buffer, two outputs (splitter).

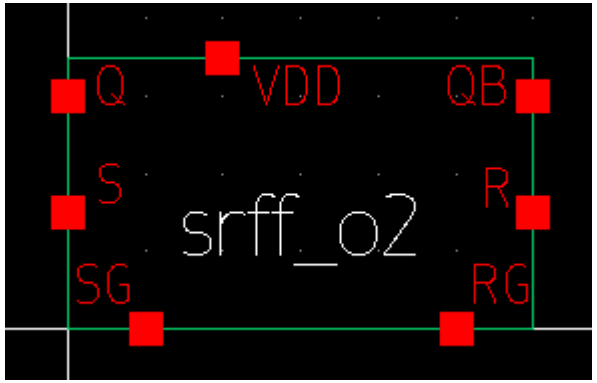




Cell: srff_o2

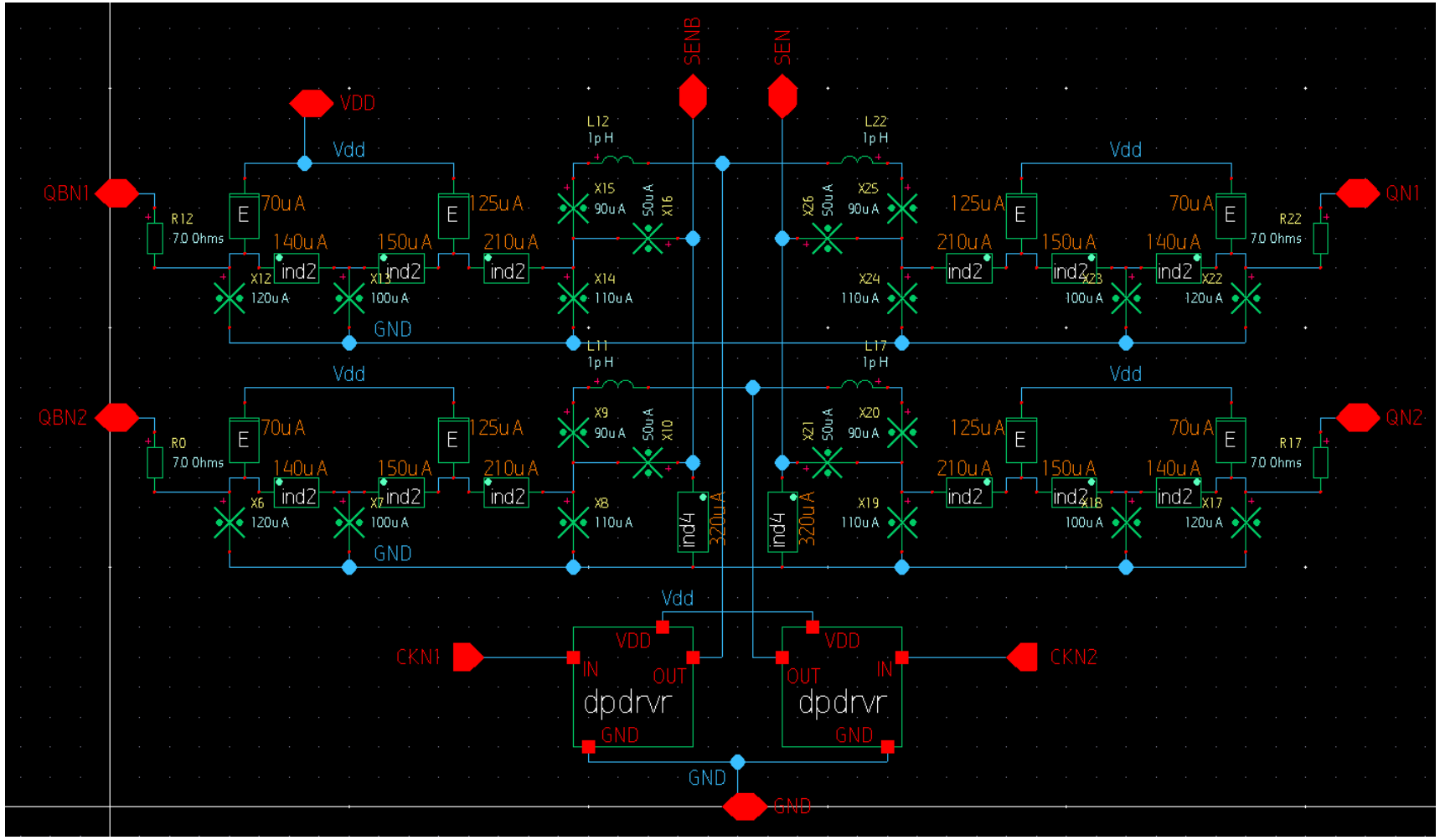
Description: S/R latch “top” subcell, with destructive unbuffered **Q** and **QB** outputs.

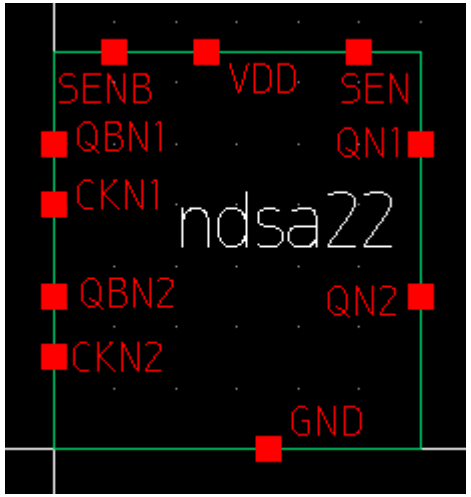




Cell: `ndsa22`

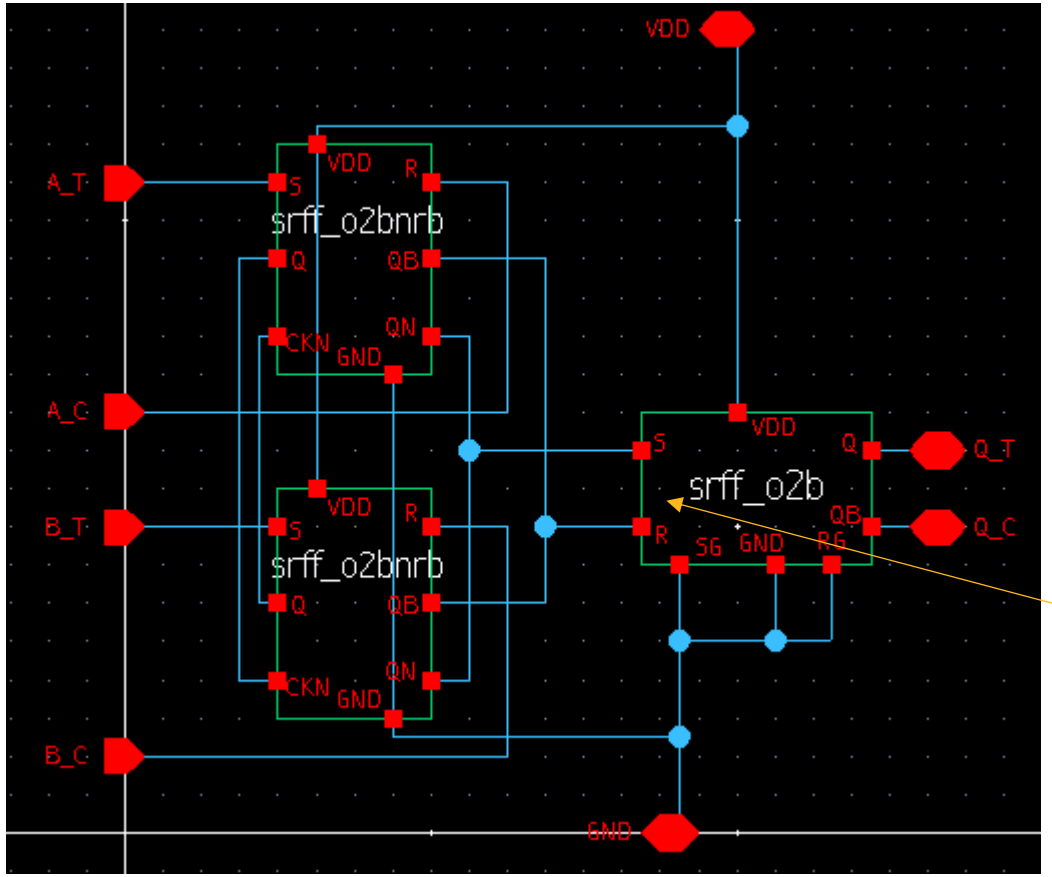
Description: non-destructive "bottom" subcell, provides two separately clocked sets of buffered **QB** and **Q** outputs.

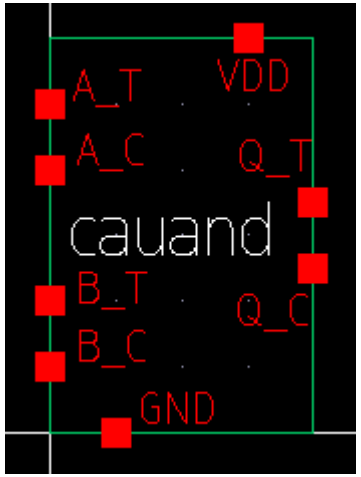




Cell: `cauand`

Description: Complementary Asynchronous universal AND gate.

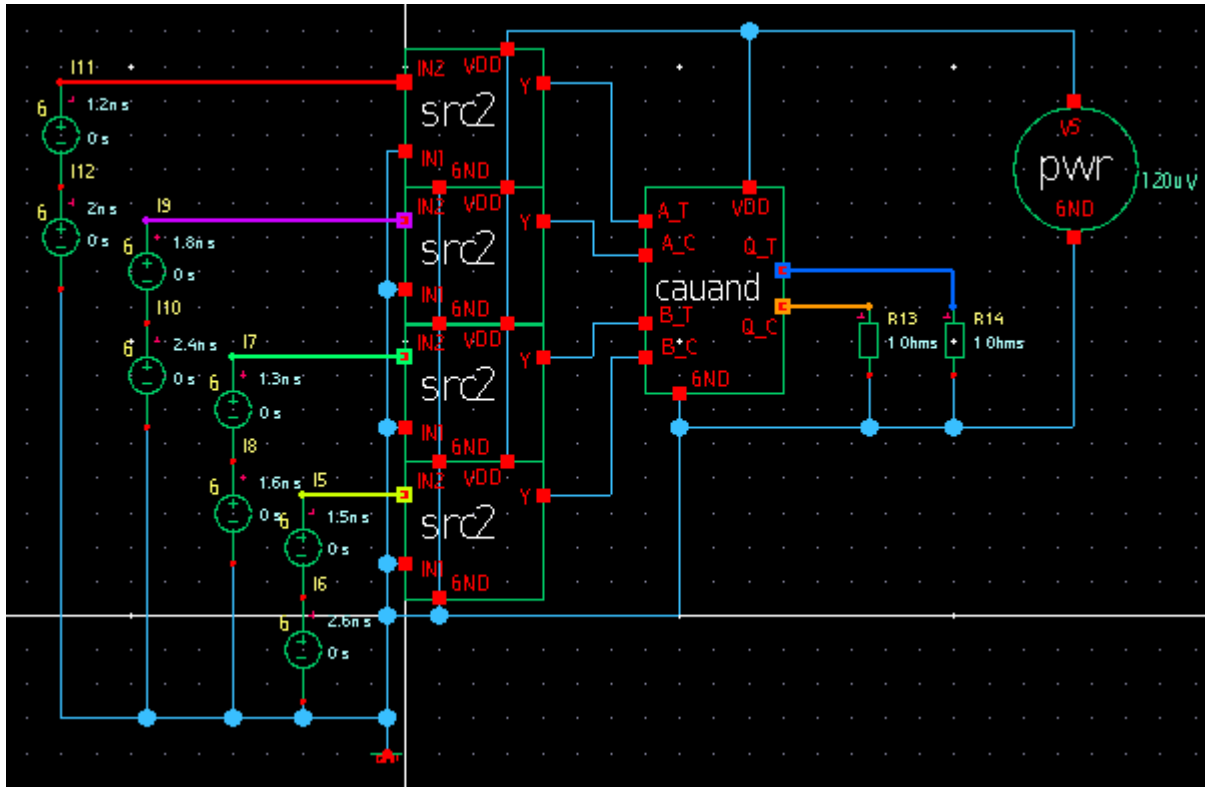


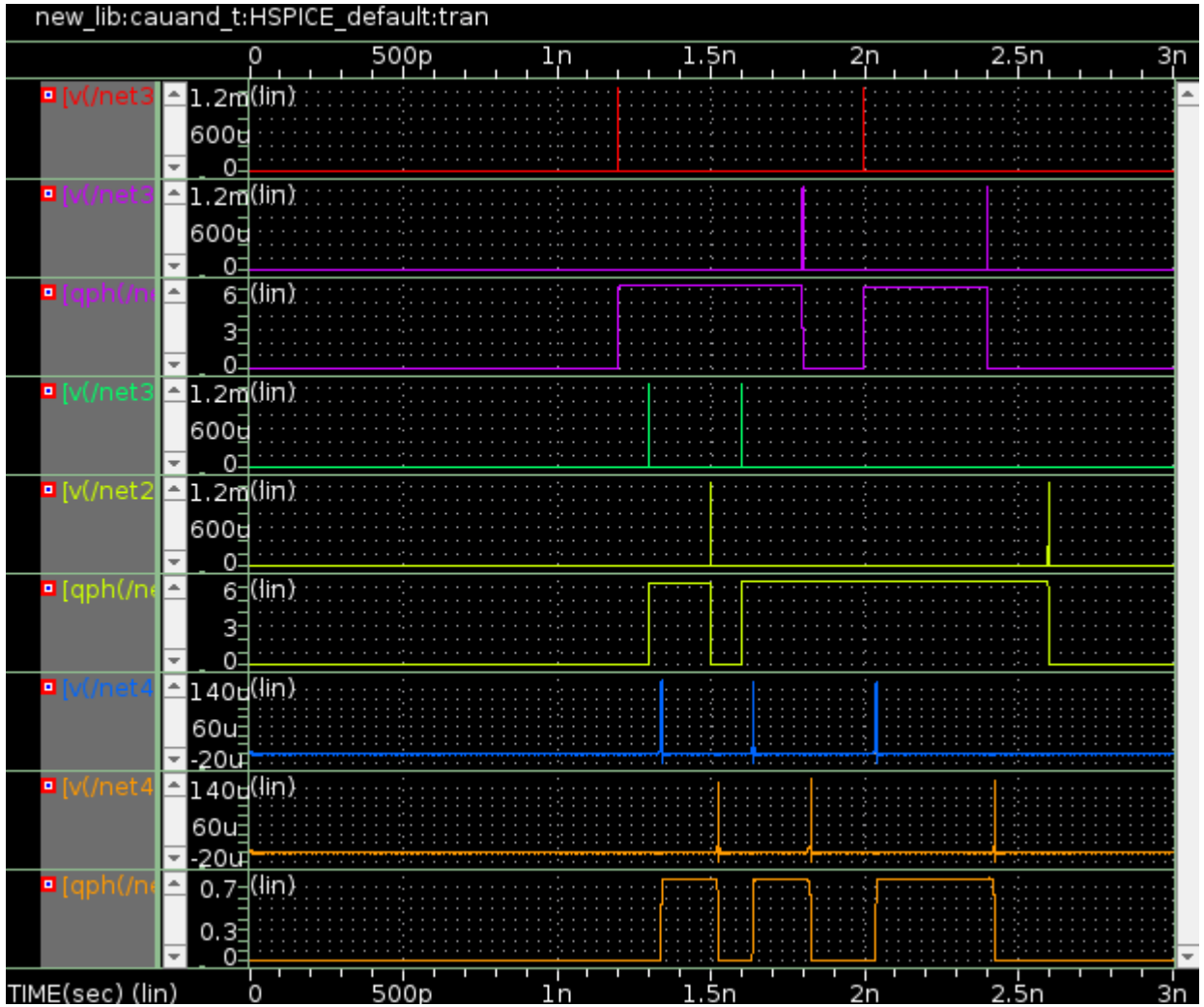


S: A -> 1 when B == 1 || B->1 when A== 1
R: A->0 || B->0

Complementary Asynchronous UAND Operation in HSPICE

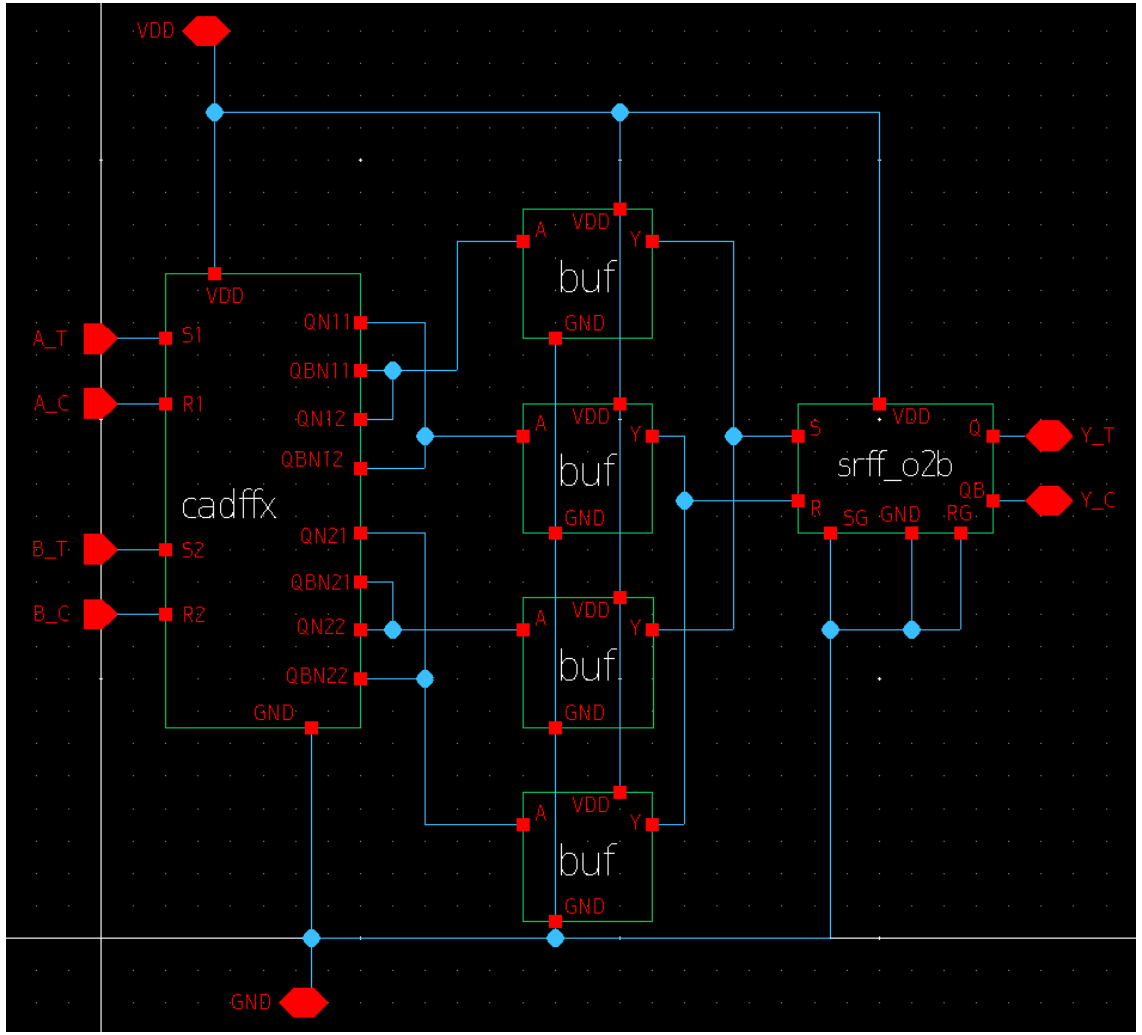
120 µV DC power for 50 GHz Clocking

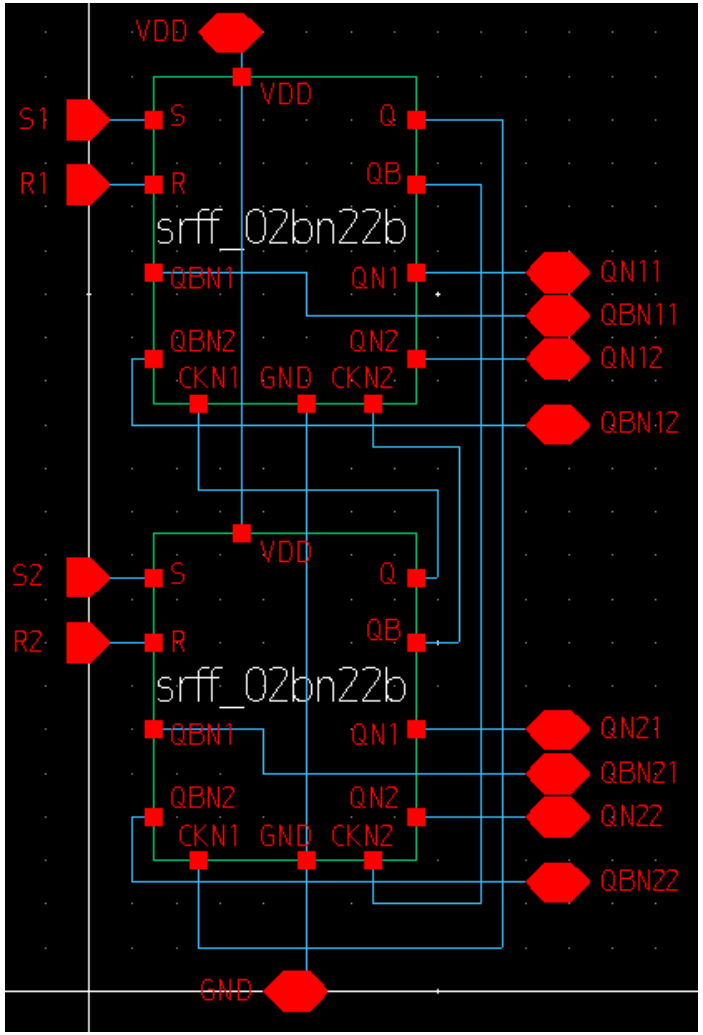




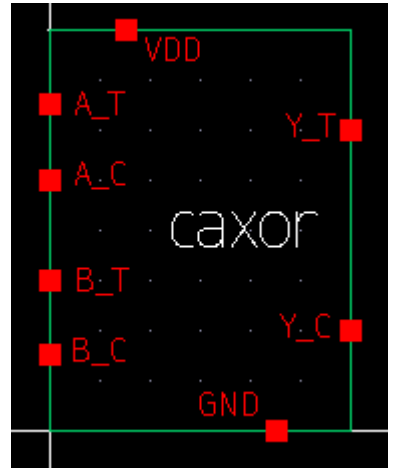
Cell: caxor

Description: Complementary Asynchronous XOR gate.



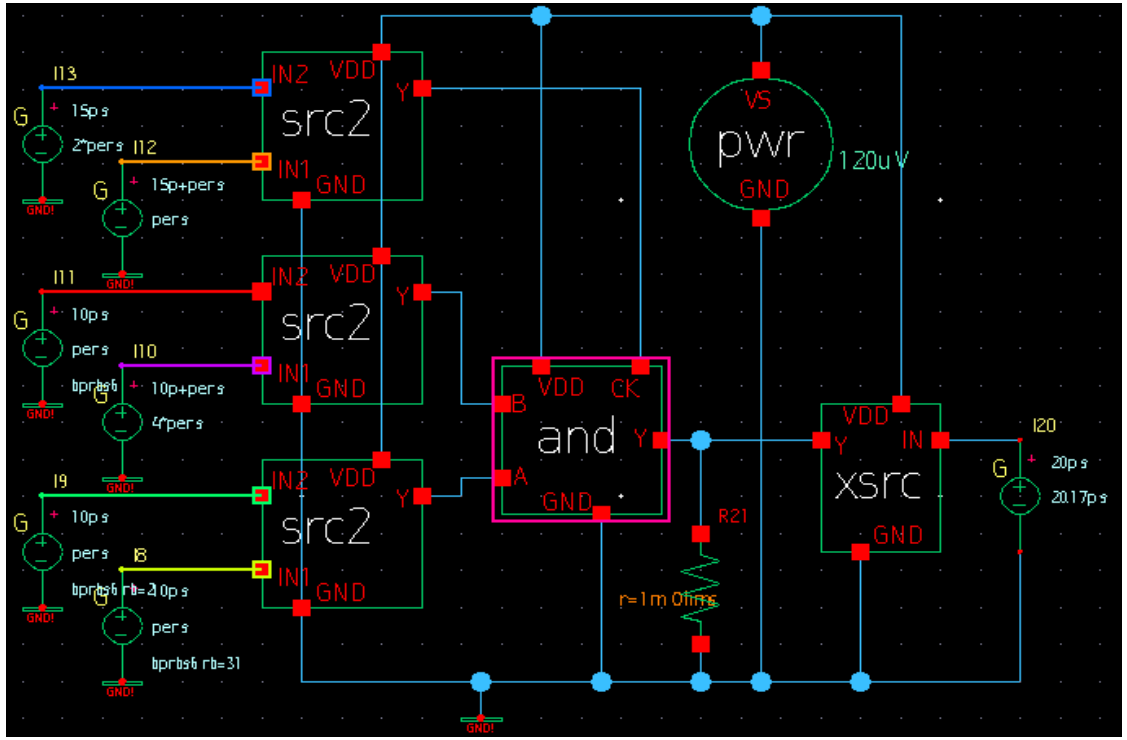


cadffx

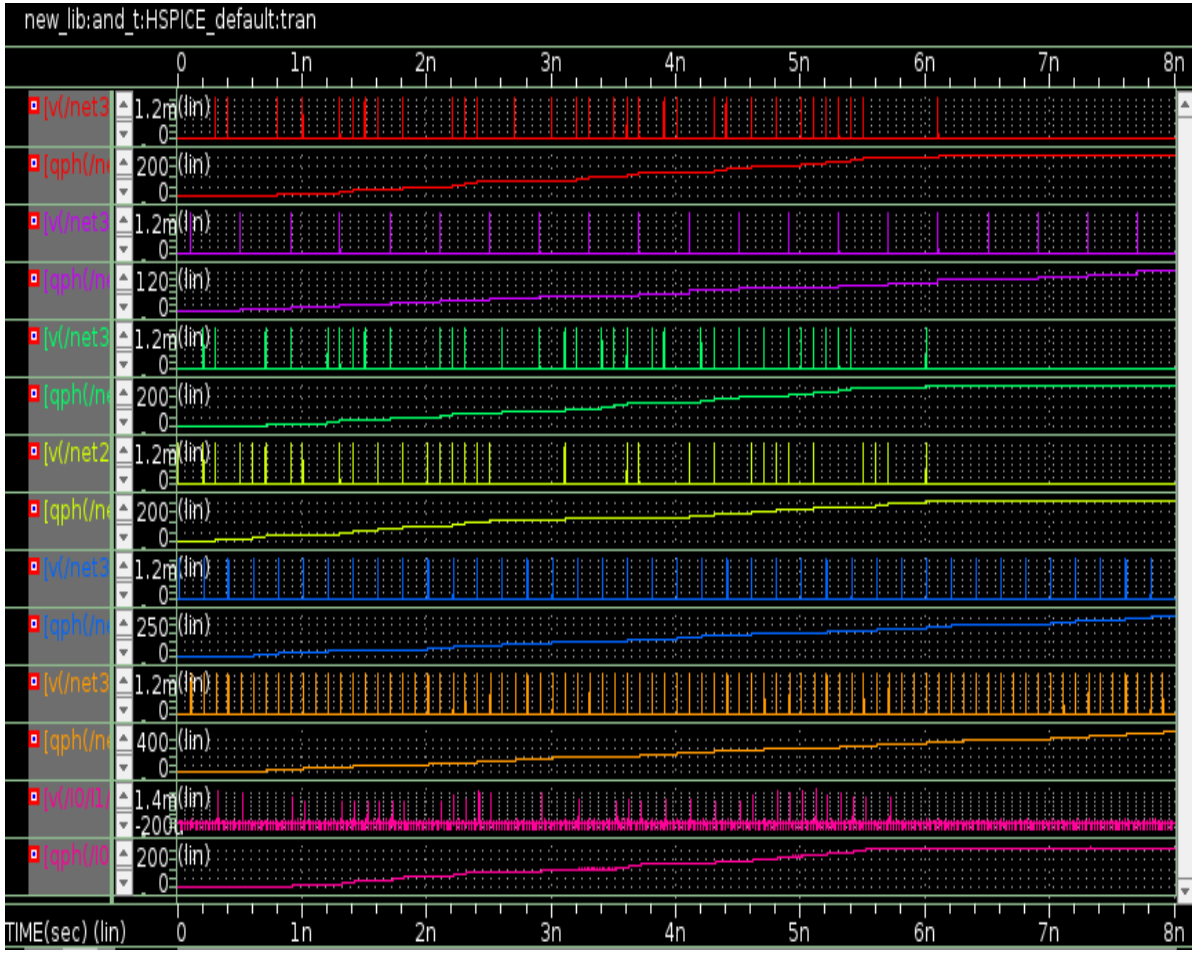


AND Gate Simulation in HSPICE

Cell **src2** wire-ORs two raw pulse sources to YSFQ input.
Cell **xsrc** provides back-propagation noise for immunity test. R21 is 0.001 ohm for shorted output test, 1K for noise immunity test.



Output is measured at output JJ, ahead of PTL damping resistor, NOT at cell output terminal.



Conclusions – Have We Met Objectives?

Density?
Need to study physical implementation. Kinetic inductor size challenge.

JJs for Inductors?
Works fine. This we could test experimentally with a regular process.

Speed?
Slightly disappointing. ~50GHz clock with certain cells, large delay in nondestructive outputs. We are close to the maximum CPIC for Nb/AlOx/Nb yet speed is not substantially better than standard 0.1 mA/μm^2. Could increase if we give up wired-OR and/or use lower impedance PTL interconnect than 16 ohms. Note that RCSJ model will lie and predict much higher speed.

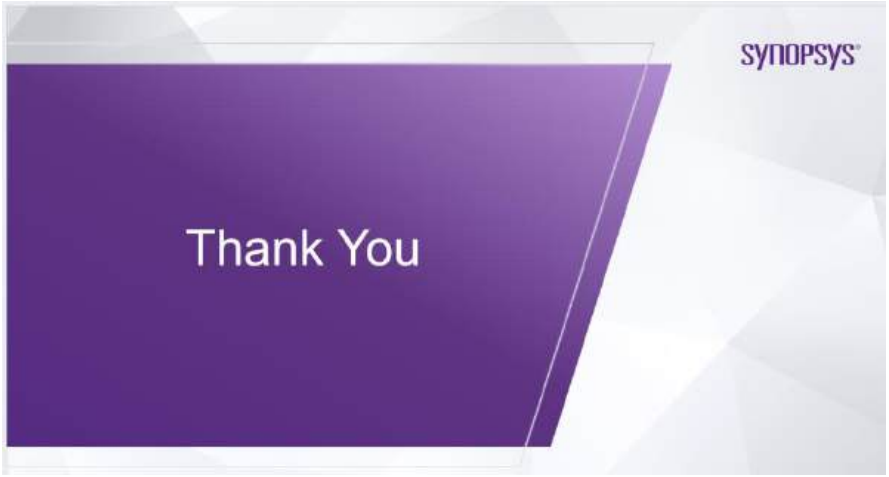
Wired OR?
Costs performance. Maybe performance is more important than density in application?

High Impedance Interconnect?
Costs performance. We could reduce impedance, maybe, with vertical transmission structures without reducing density, in which case we can probably gain back some performance.

Conclusions, Continued

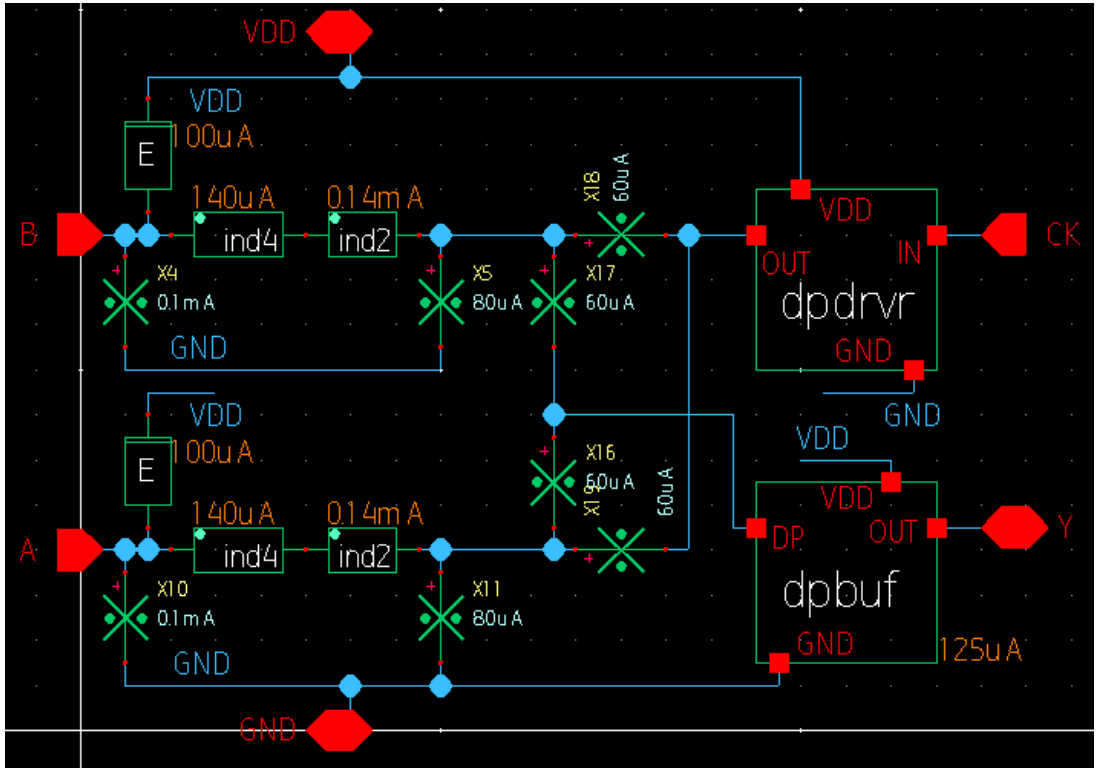
From 2EOr2B-06
Technical Challenge: How to interface self-shunted JJ's to advanced-node cryo-CMOS? We need a 2.6 mV step source, self-shunting makes this difficult.

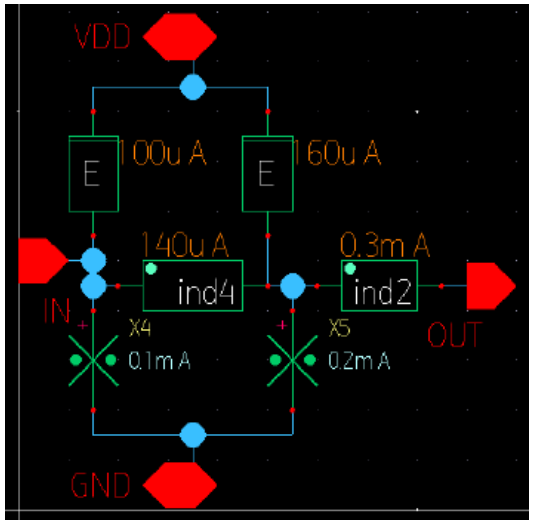
Solving this problem is important, as CMOS integration may be the likely usage modality for SFQ in general. This will be addressed in future work at Synopsys.



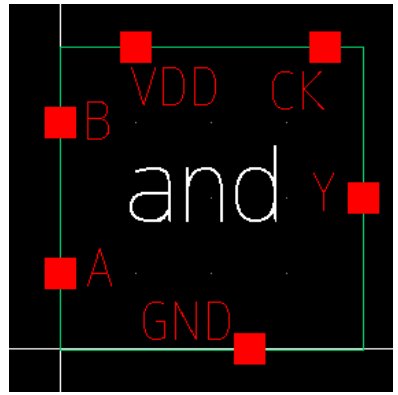
Thank You

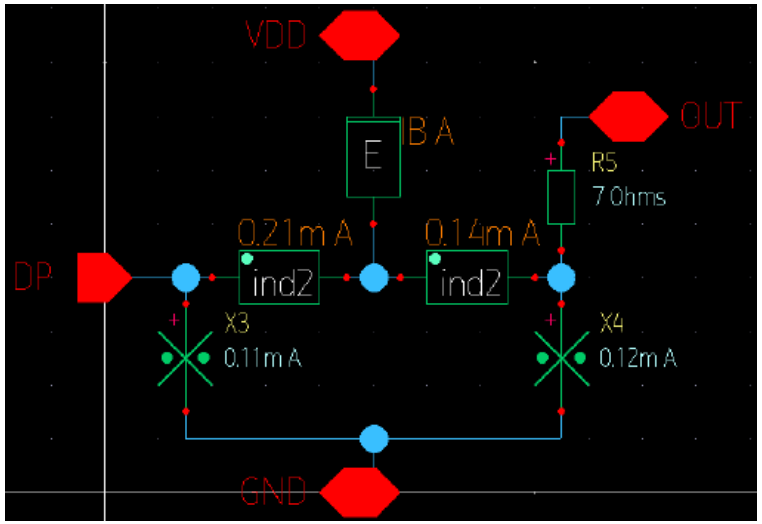
AND Gate Schematic





dpdrvr

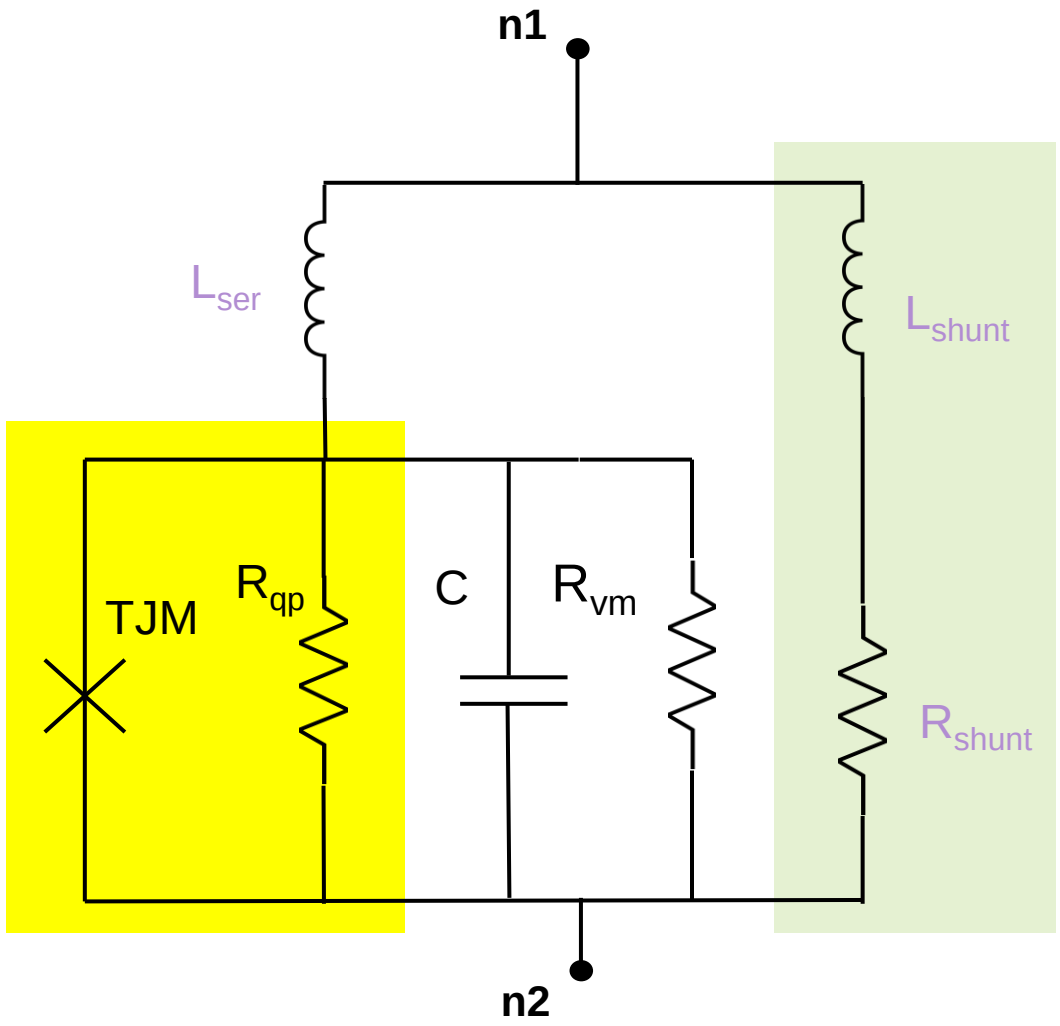




dpbuf

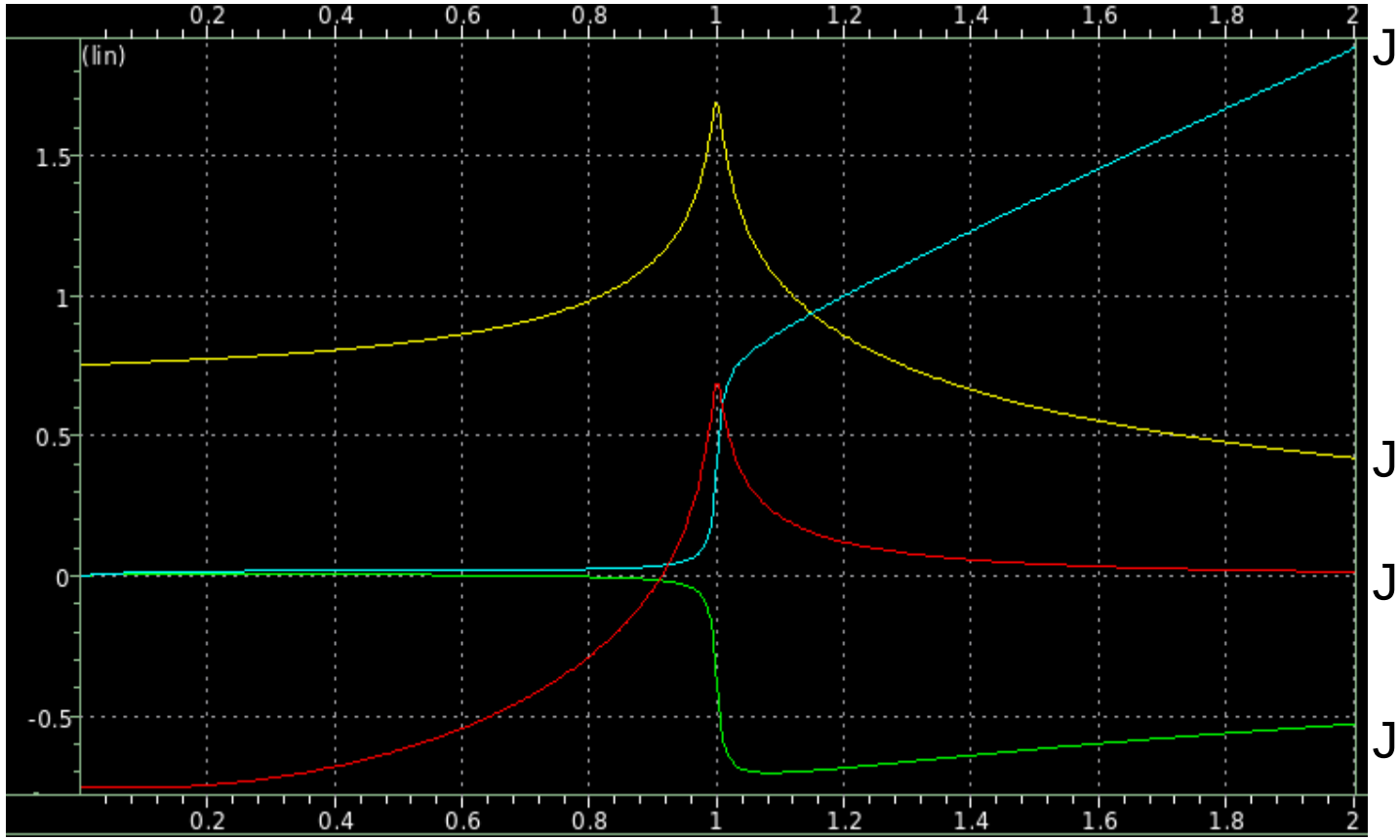
Compact Tunnel Junction Model Schematic

- Yellow highlighting indicates pair and quasiparticle transport from TCA tables, temperature adjusted I_c.
- Green highlight indicates optional R_{shunt} and L_{shunt} external shunt resistor with series inductance.
- L_{ser} models series inductance.
- Geometric capacitance is handled explicitly.
- R_{vm} adds additional conductance to supplement R_{qp} and obtain specified V_m (product of sub-gap resistance and critical current).



Tunnel Current Amplitudes From ***mmjco*** Can Be Plotted

Synopsys *WaveView*



Jqp_imag

Jpair_real

Jqp_real

Jpair_imag

- Files use SPICE “rawfile” format.
- Jqp_imag dominates quasiparticle current.
- Jpair_real dominates pair current.
- Other terms produce “anomalous” phase shifts.
- Riedel peak at gap.