Workshop on Detection and Mitigation of Flux Trapping
in Superconducting Digital Electronics

AIST
Create the Future, Collaborate Together

Superconducting digital circuits fabrication process at AIST

Qufab
G-QuAT

2024/12/13

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Global Research and Development Center for Business by Quantum-AI Technology (G-QuAT)
National Institute of Advanced Industrial Science and Technology (AIST)

Outline

- Introduction of fabrication facility at AIST (Qufab)
- Superconducting digital circuits and their fabrication process
- Recent results at Qufab
- Qufab foundry service
- Summary

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Qufab: Superconducting Quantum Circuit Fabrication Facility

- CR size：720m^2, CR class：1000（partially 100）
- 4-inch line (partially compatible with 3-inch)
- Over 70 equipment

Qufab: Superconducting Quantum Circuit Fabrication Facility

AIST
Create the Future, Collaborate Together

◆History of our fabrication facility

2012 CRAVITY

(Clean Room for Analog & digital superconductiVITY)

- CRAVITY was a facility for prototyping superconducting digital and analog circuits.
- 3-inch line

2022 Qufab

（Superconducting Quantum Circuit Fabrication Facility）

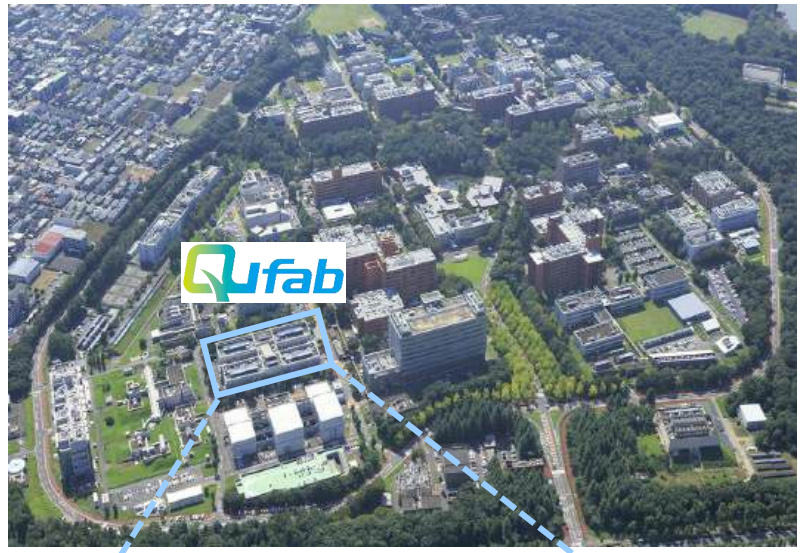
- **Qufab was started in 2022 as a renewal of CRAVITY.**
  - ✓ **Establishment of 4-inch line**
  - ✓ 27 process and measurement equipment were replaced.
  - ✓ Available: superconducting circuit, qubit, 3-D integration

2023/7 G-QuAT established

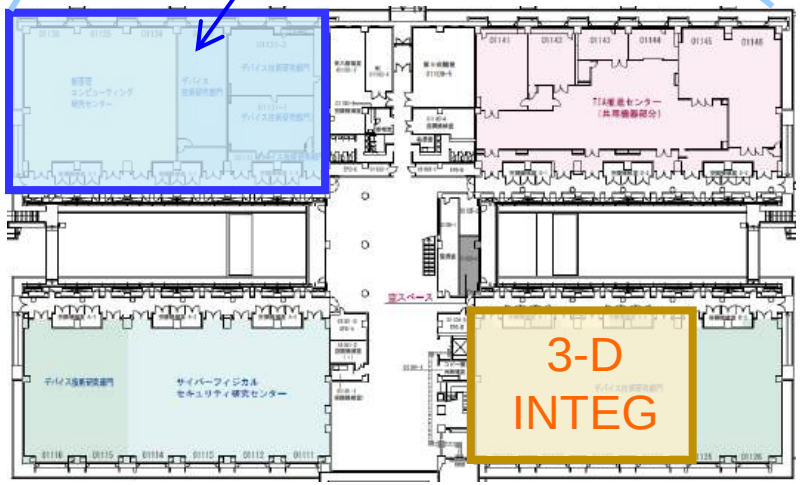
（Global Research and Development Center for Business by Quantum-AI technology）

➢ Support implementation of quantum technology to social society

AIST, Tsukuba



Superconducting circuits, quantum circuits



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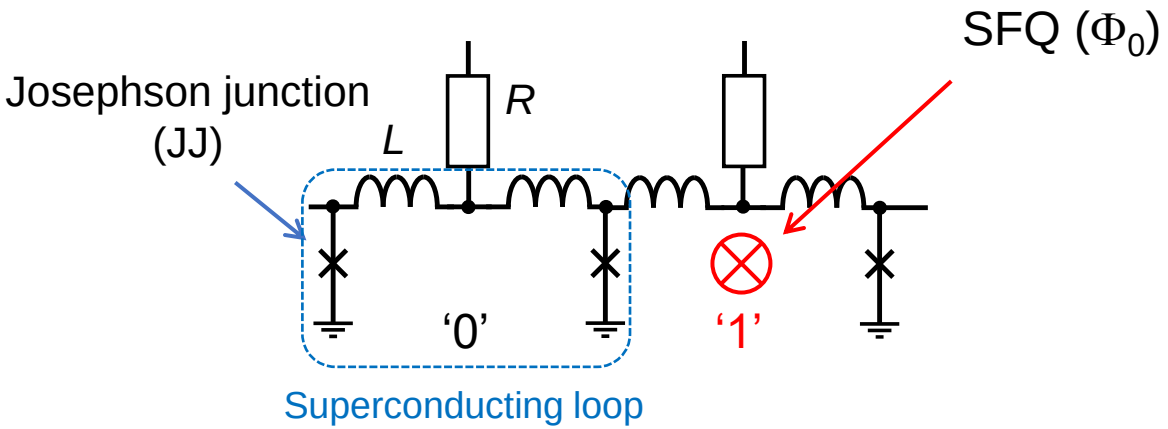
Superconducting digital circuits

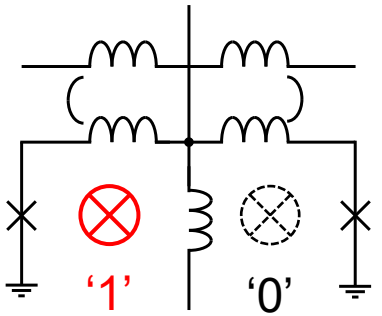
- Single-flux-quantum circuit (SFQ)



Logic state is determined based on whether there is an SFQ in a superconducting loop.

- ✓ High-speed operation (~ 100 GHz)
- ✓ Asynchronous operation (event-driven)

- Adiabatic quantum-flux-parametron (AQFP)



Logic state is determined based on which of two loops has an SFQ.

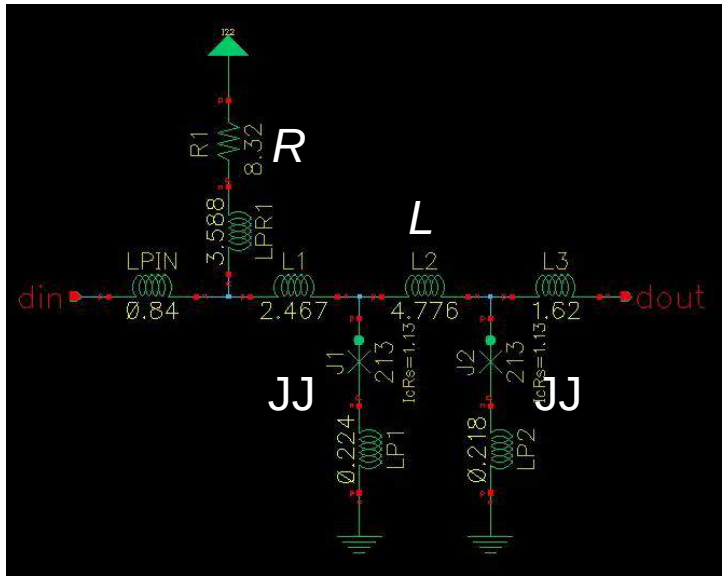
- ✓ Extremely low-power consumption
- ✓ Low current driven (~mA)

➢ Both circuit components: Josephson junction (JJ), inductor (*L*), resistor (*R*)

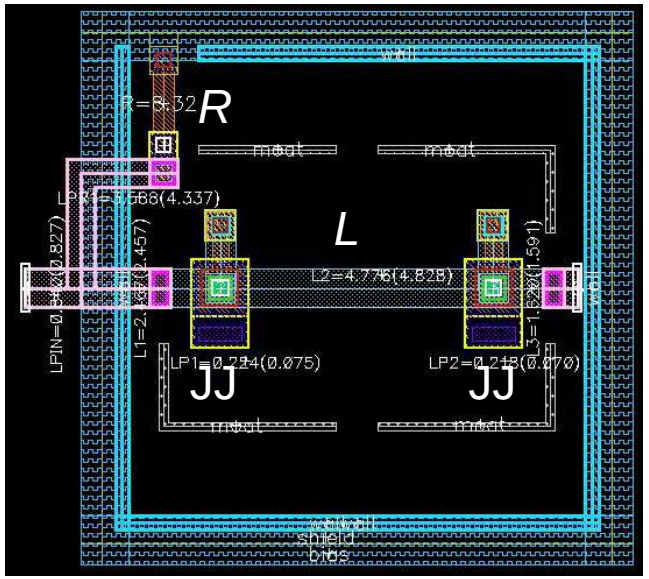
Cell library

◆ JTL (Josephson transmission line) cell contents

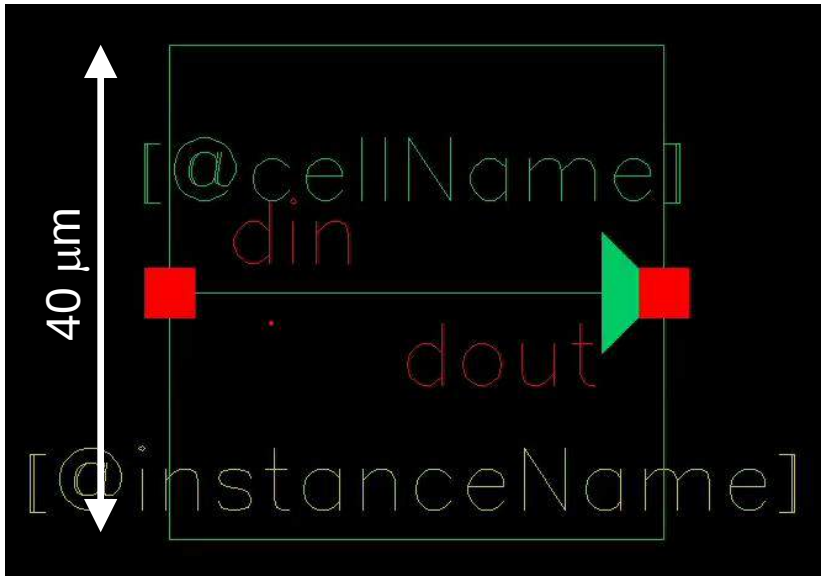
Circuit schematic



Physical layout



Symbol



- Various JTLs, logic circuits (DFF, OR, …) are made into cells and stored in libraries (cell library). Large-scale circuits can be designed by arranging cells like a puzzle.

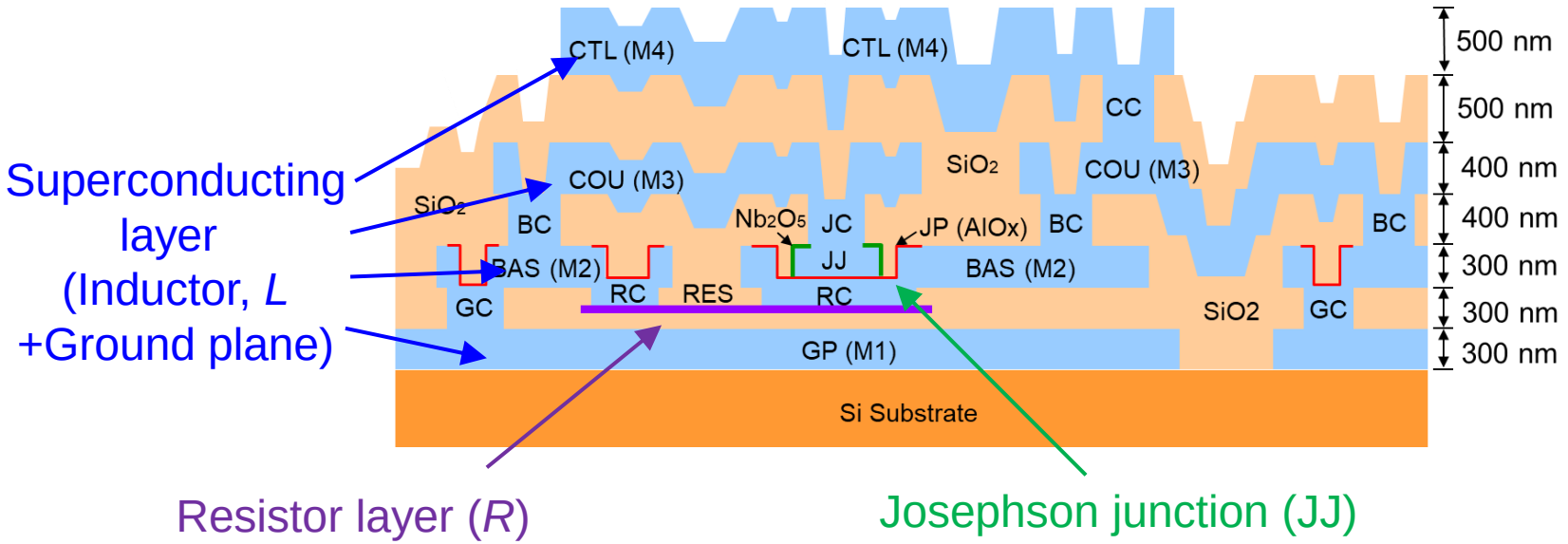
➢ In Japan:

- SFQ cell library which contain **over 300 cells**, called CONNECT cell library, was developed [1].
- AQFP cell library: only **~ 40 cells** are needed to design large-scale circuits by adopting minimalist design [2].

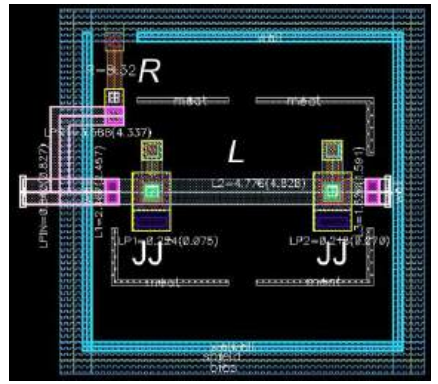
[1] S. Yorozu, *Physica C supercond.*, 2002. [2] N. Takeuchi, *J. Appl. Phys.*, 2015.

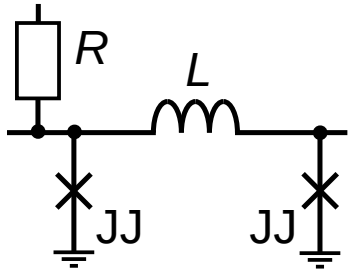
Fabrication process for superconducting digital circuits

Device structure of standard process with 4-Nb layers (HSTP)



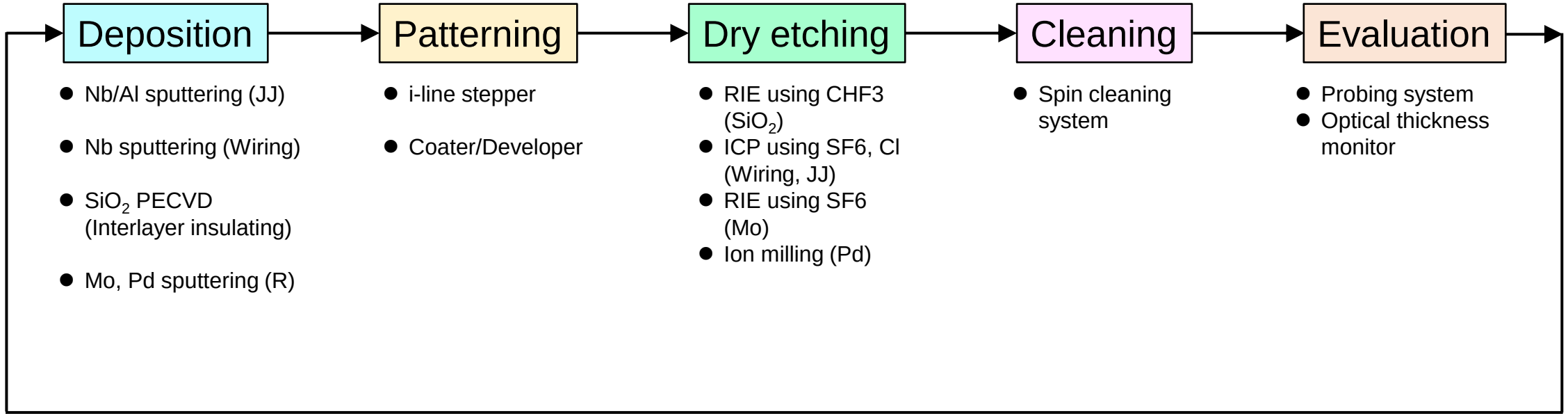
Circuit design (JTL)





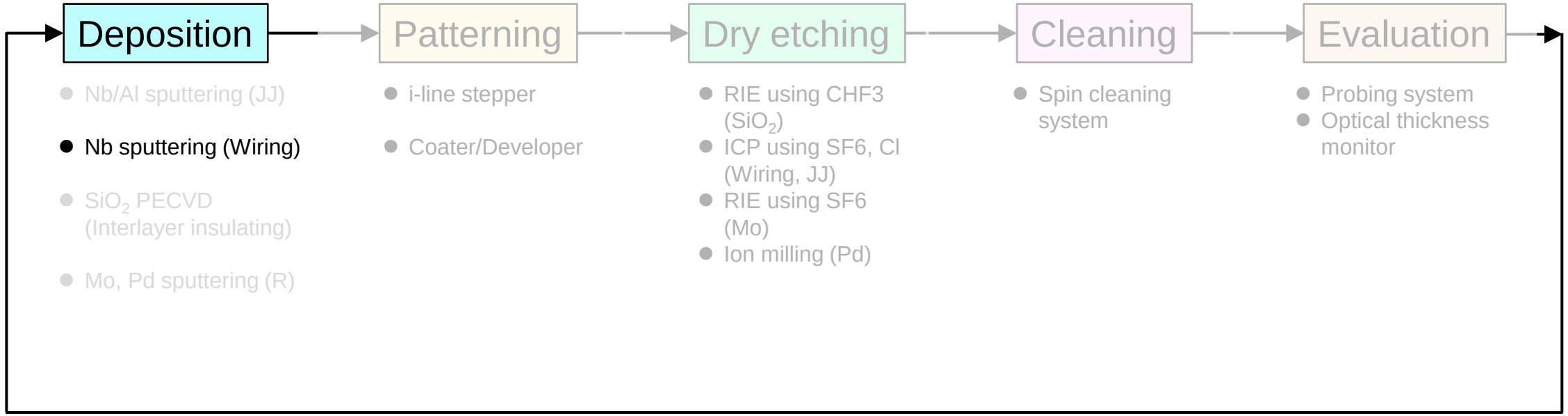
- JJ: Nb/Al-AlOx/Nb, Wiring: 4 Nb layers, Resistor: Usually Mo (Pd for millikelvin temperature)
- Fabrication process determine the main parameters ($L_{\square}$, $R_{\square}$, and J_c (critical current density of JJ)) and provide the design rules linked to the process equipment and conditions.
- Precise, stable control of circuit parameters through the fabrication process is important for the development of large-scale superconducting circuits.

Main steps and equipment in the fabrication process

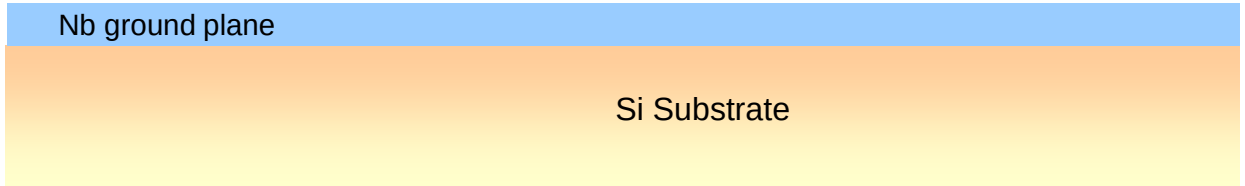


Si Substrate

Main steps and equipment in the fabrication process



1. Deposition of Nb film



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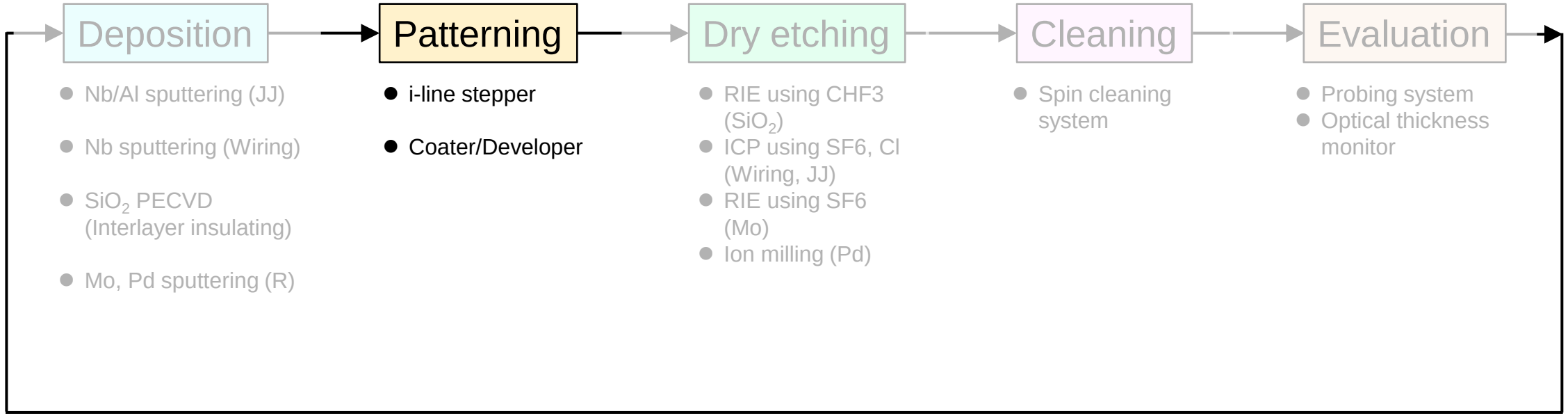
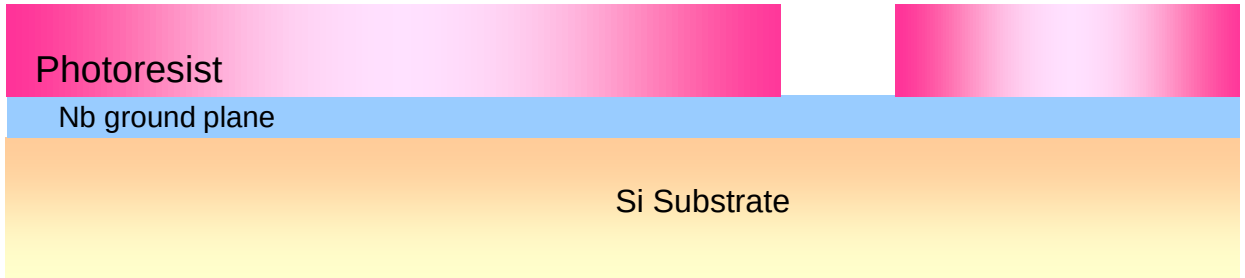


1. Deposition of Nb film
2. Patterning using photolithography



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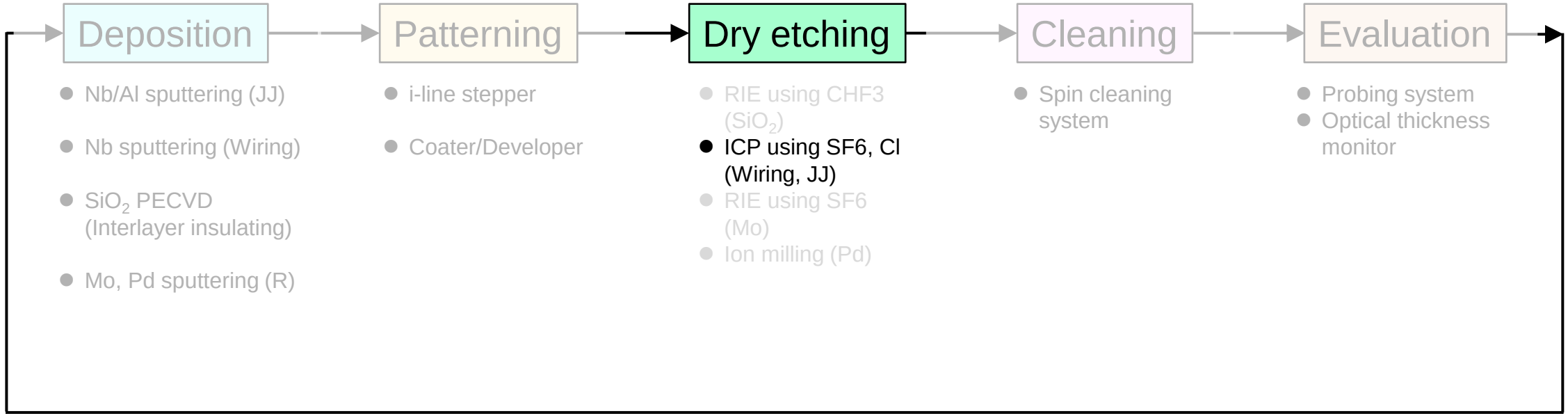
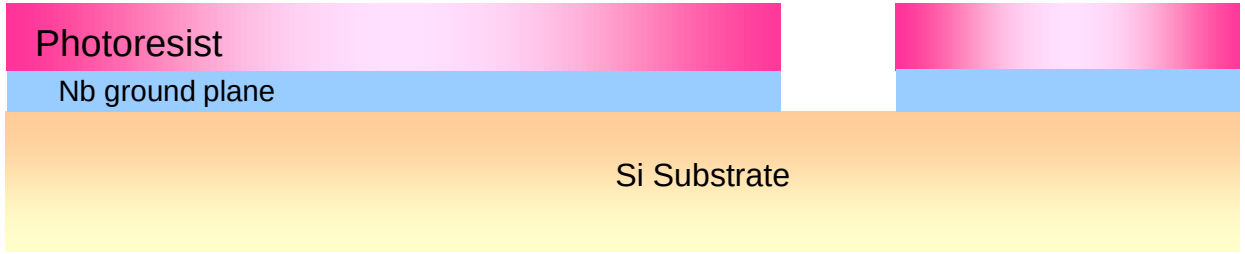
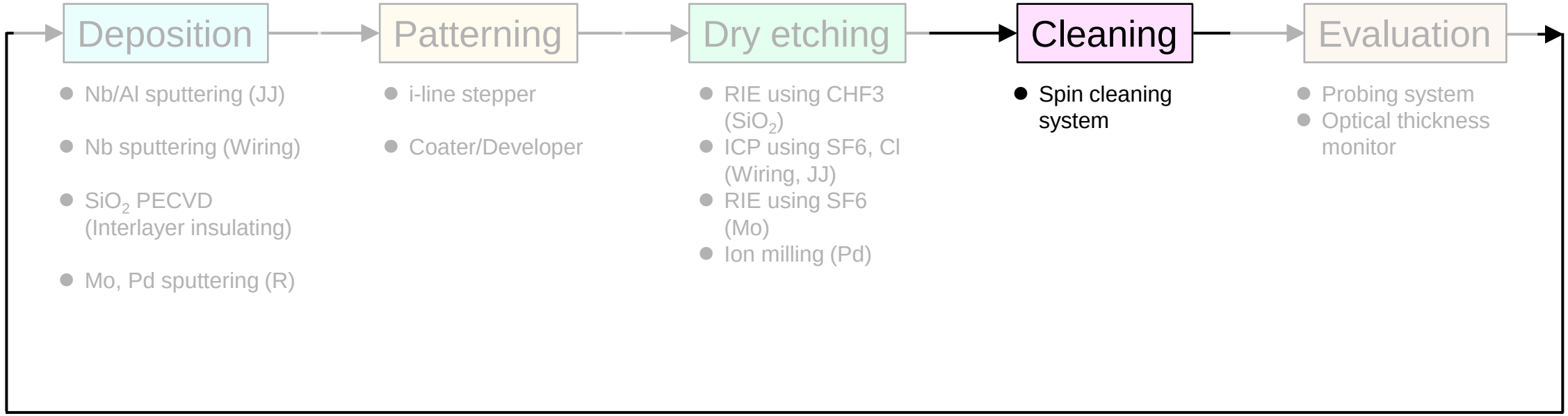


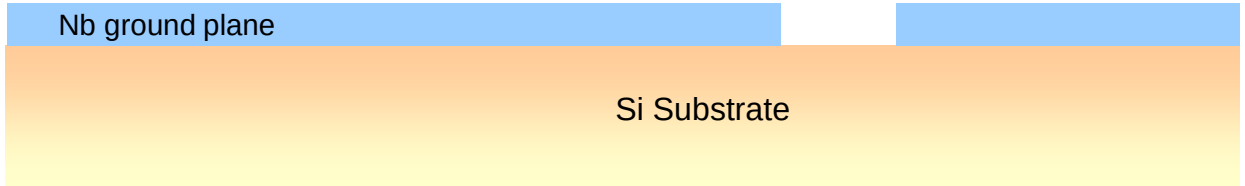
1. Deposition of Nb film
2. Patterning using photolithography
3. Pattern transfer by etching



Main steps and equipment in the fabrication process



1. Deposition of Nb film
2. Patterning using photolithography
3. Pattern transfer by etching
4. Removing the residual photoresist



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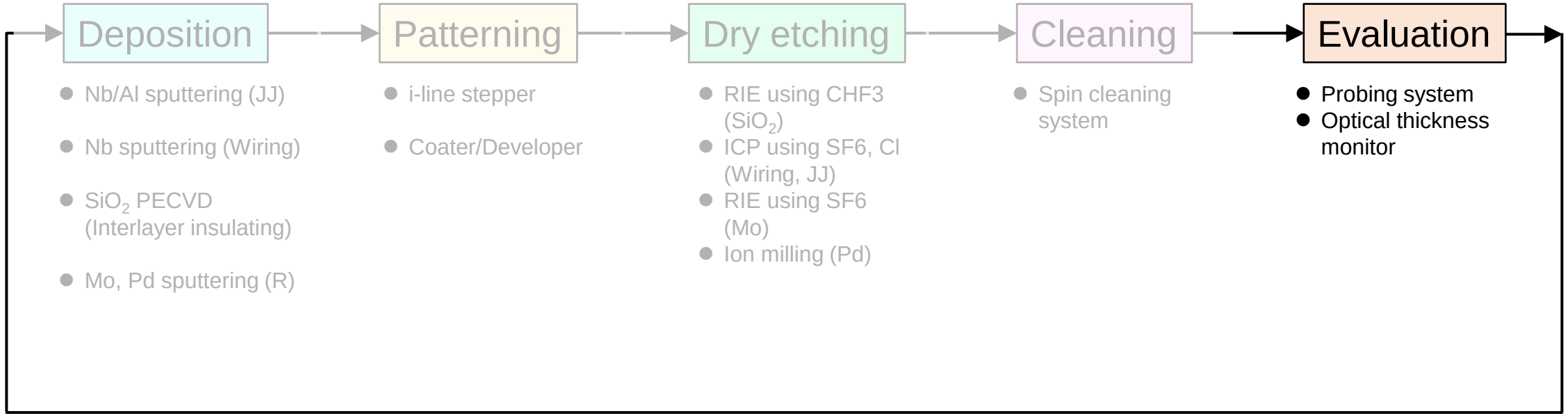
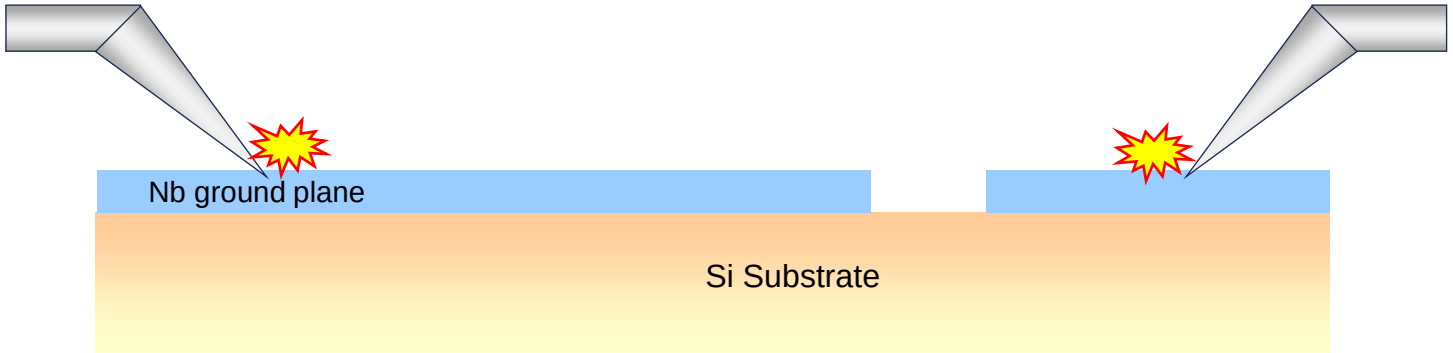
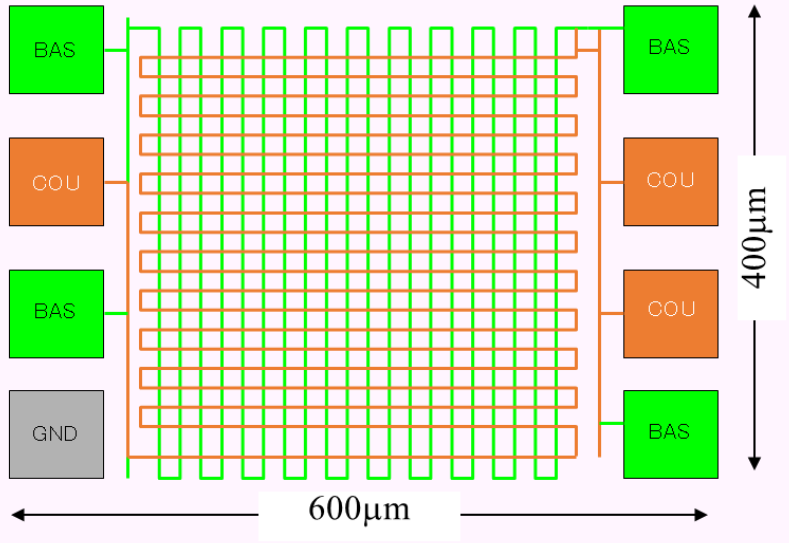


1. Deposition of Nb film
2. Patterning using photolithography
3. Pattern transfer by etching
4. Removing the residual photoresist
5. Probing diagnostic chips at room temp.



Main steps and equipment in the fabrication process

Example of diagnostic pattern



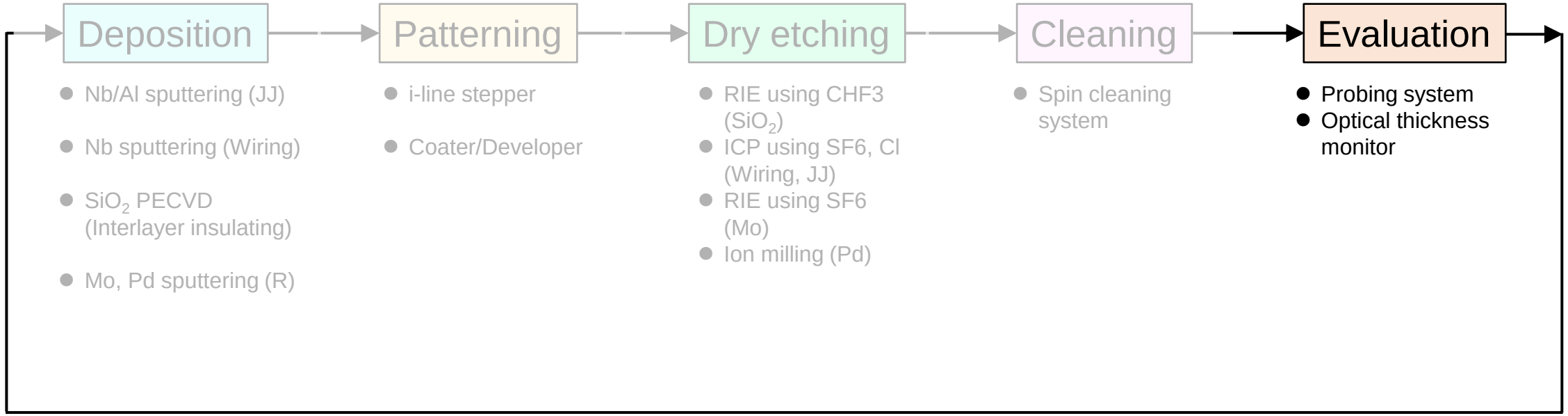
Measure meander patterns that cross multiple layers and check for short circuits or breaks

4-inch wafer shot map

	A	B	C	D	E	F	G	H	I	J	K	L
				C8	C8	C8	C8	C8	C8			
1			C8	C8	C1	C4	C5	C1	C4	C5	C8	C8
2		C8	C8	C6	C2	C8	C6	C2	C8	C6	C2	C8	C8	
3		C8	C9	C7	C3	C9	C7	C3	C9	C7	C3	C9	C8	
4	C8	C1	C4	C5	C1	C4	C5	C1	C4	C5	C1	C4	C5	C8
5	C8	C2	C8	C6	C2	C8	C6	C2	C8	C6	C2	C8	C6	C8
6	C8	C3	C9	C7	C3	C9	C7	C3	C9	C7	C3	C9	C7	C8
7	C8	C1	C4	C5	C1	C4	C5	C1	C4	C5	C1	C4	C5	C8
			C8	C6	C2	C8	C6	C2	C8	C6	C2	C8	C6	C8
9	C8	C3	C9	C7	C3	C9	C7	C3	C9	C7	C3	C9	C7	C8
10		C8	C4	C5	C1	C4	C5	C1	C4	C5	C1	C4	C8	
11		C8	C8	C6	C2	C8	C6	C2	C8	C6	C2	C8	C8	
12			C8	C8	C3	C9	C7	C3	C9	C7	C8	C8		
					C8	C8	C8	C8	C8	C8				

Pink: diagnostic chip
Blue: circuit chip

Main steps and equipment in the fabrication process



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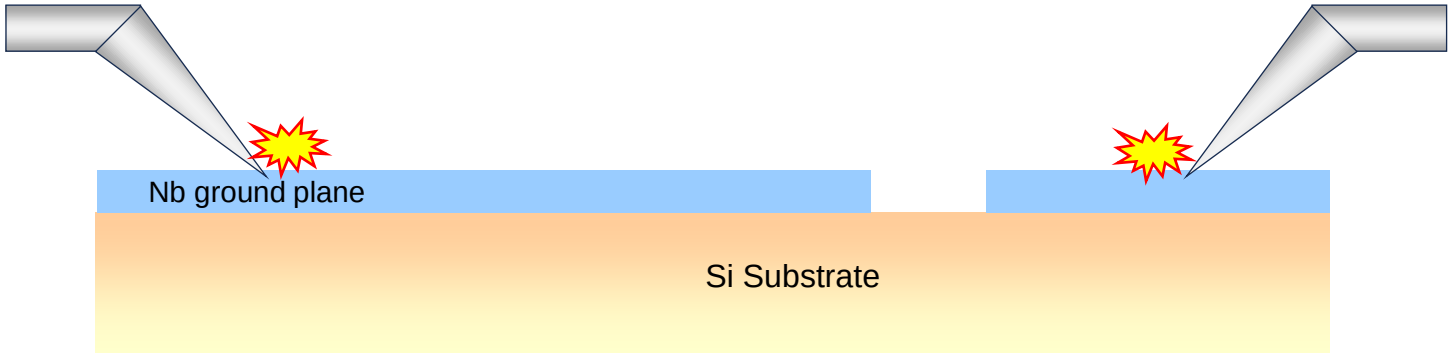

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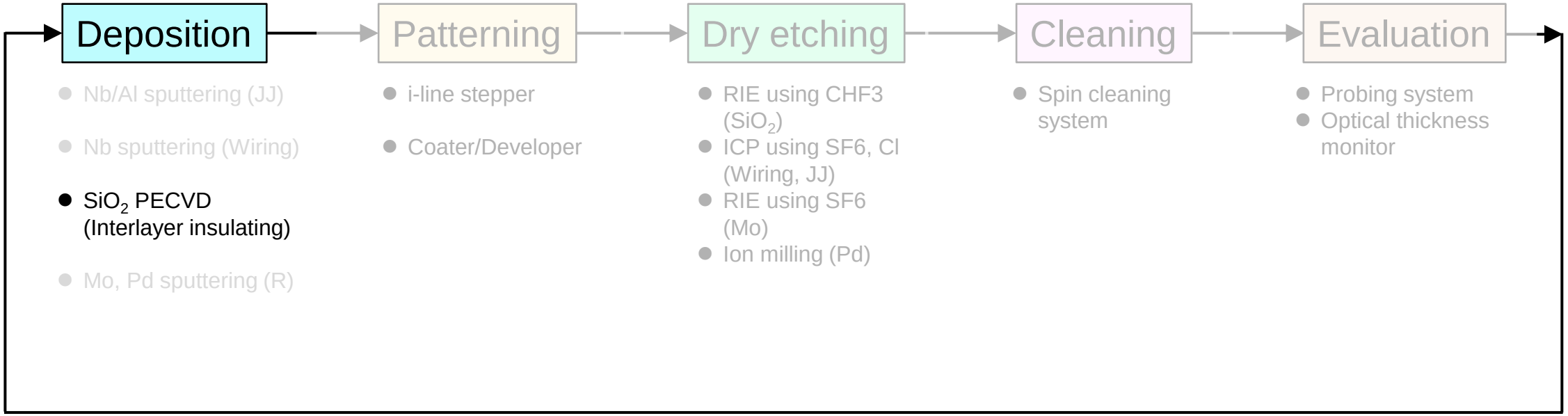

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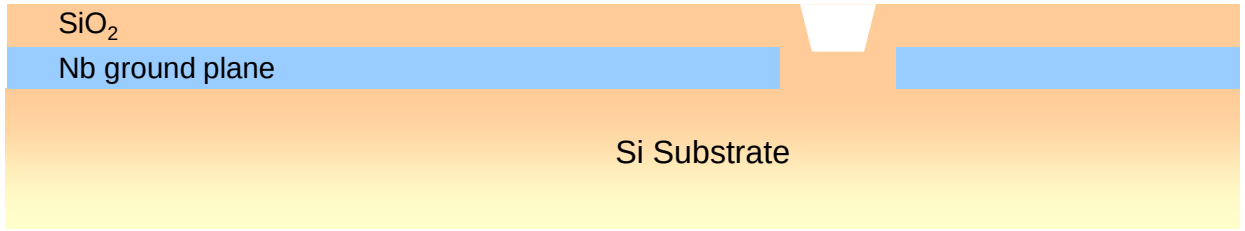

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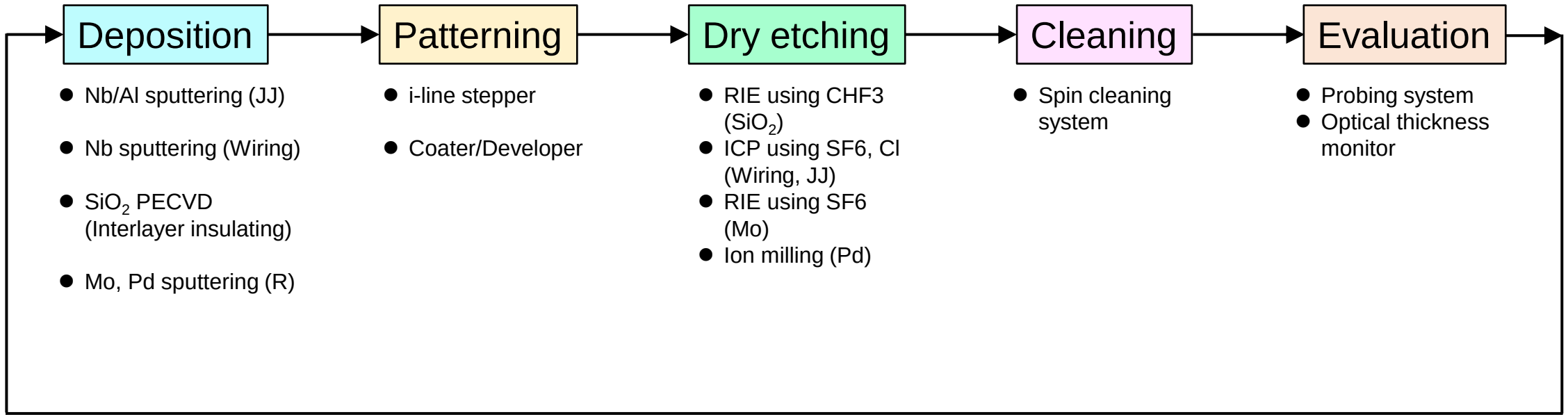
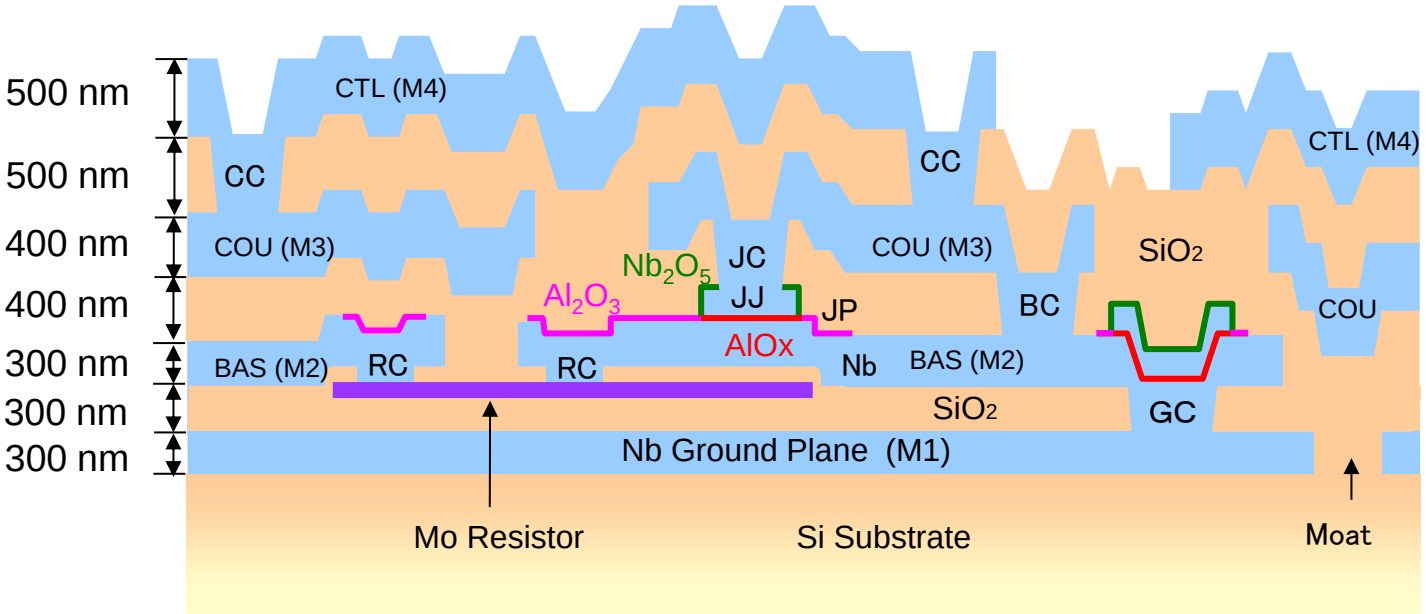
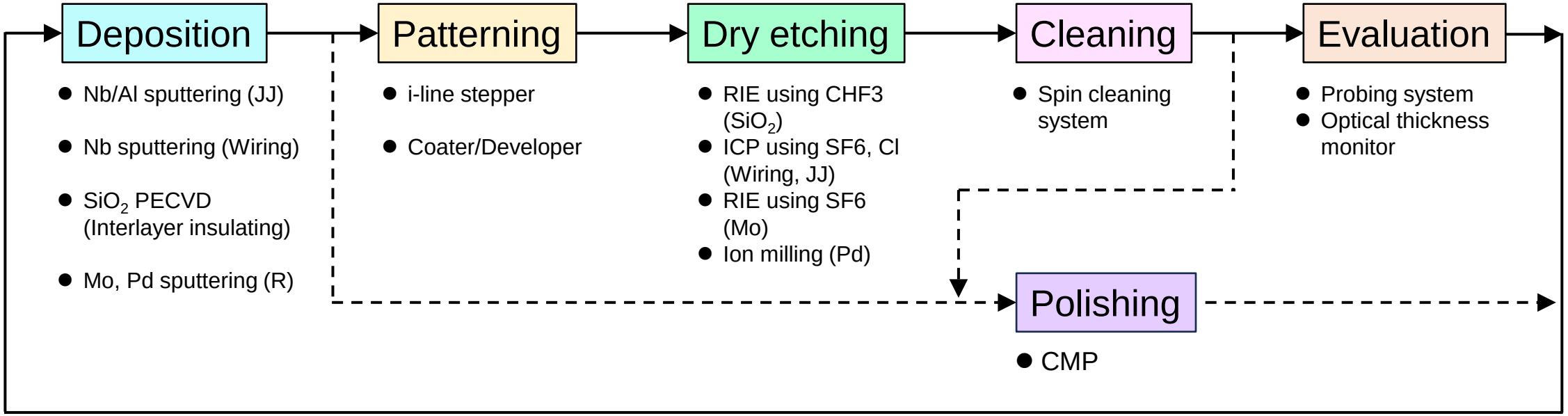




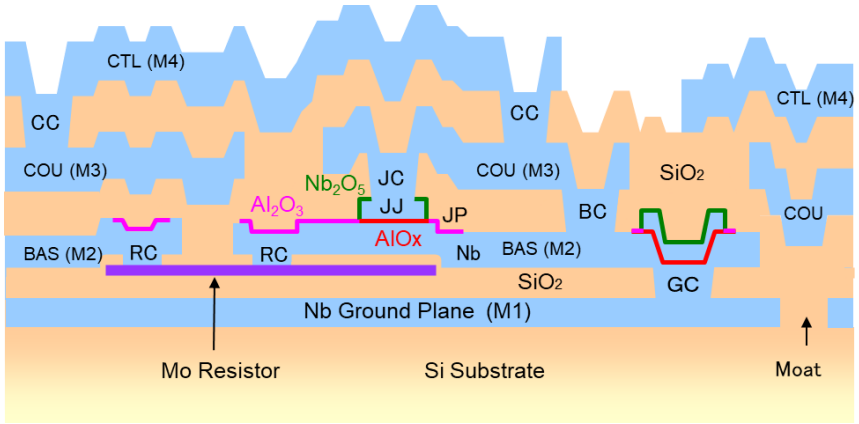
◆ Standard process (HSTP)

- Nb 4 layers including GP
- J_c: 10 kA/cm^2
- $R_\square$(Mo): 2.4 Ω
- Minimum line width: 1 μm
- Processing steps: ~ 150

Main steps and equipment in the fabrication process

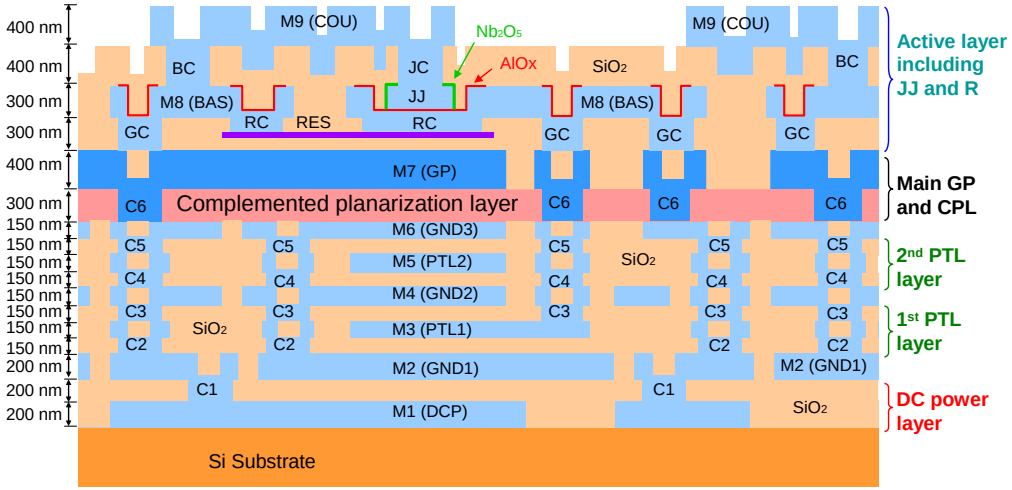


Nb 4-layers, HSTP

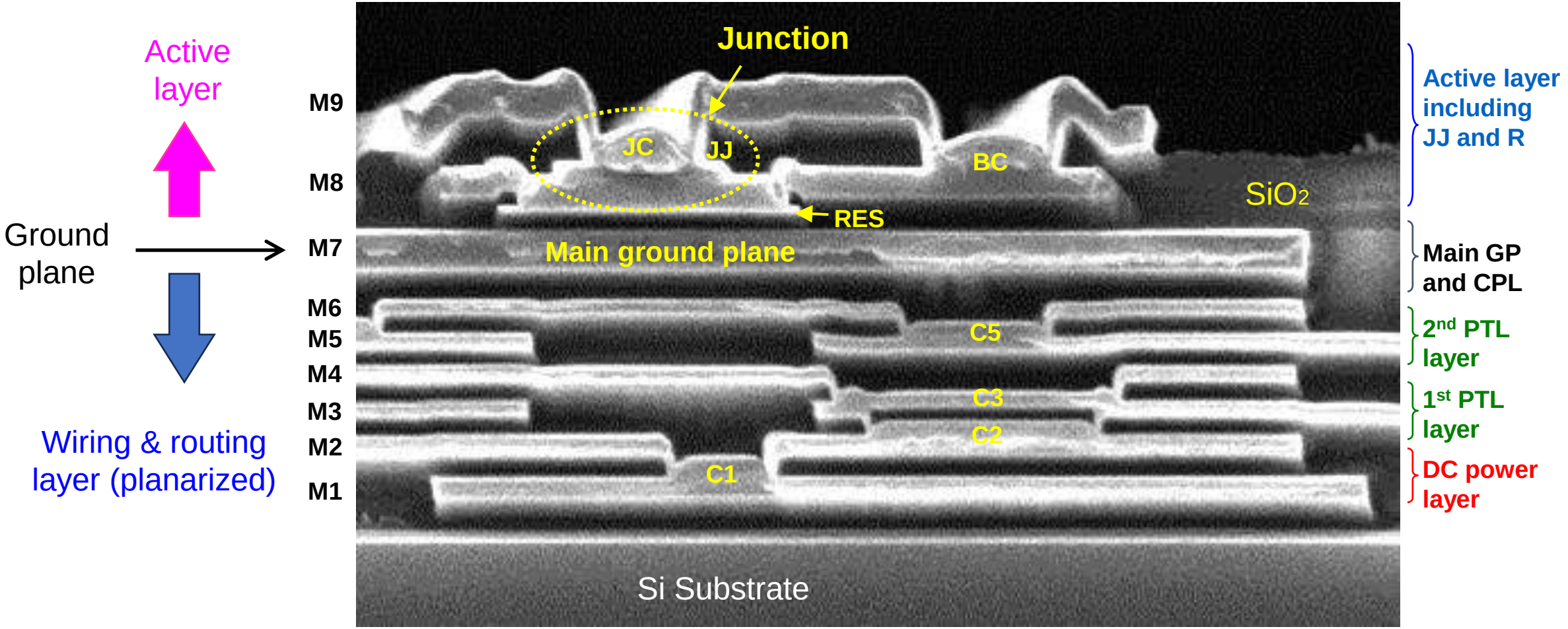


More multi-layer…

Nb 9-layers, ADP (partially planarized)



Cross-sectional SEM photograph of Nb 9-layer device structure



Excellent flatness was obtained even though the step edges of several underlying patterns are included.

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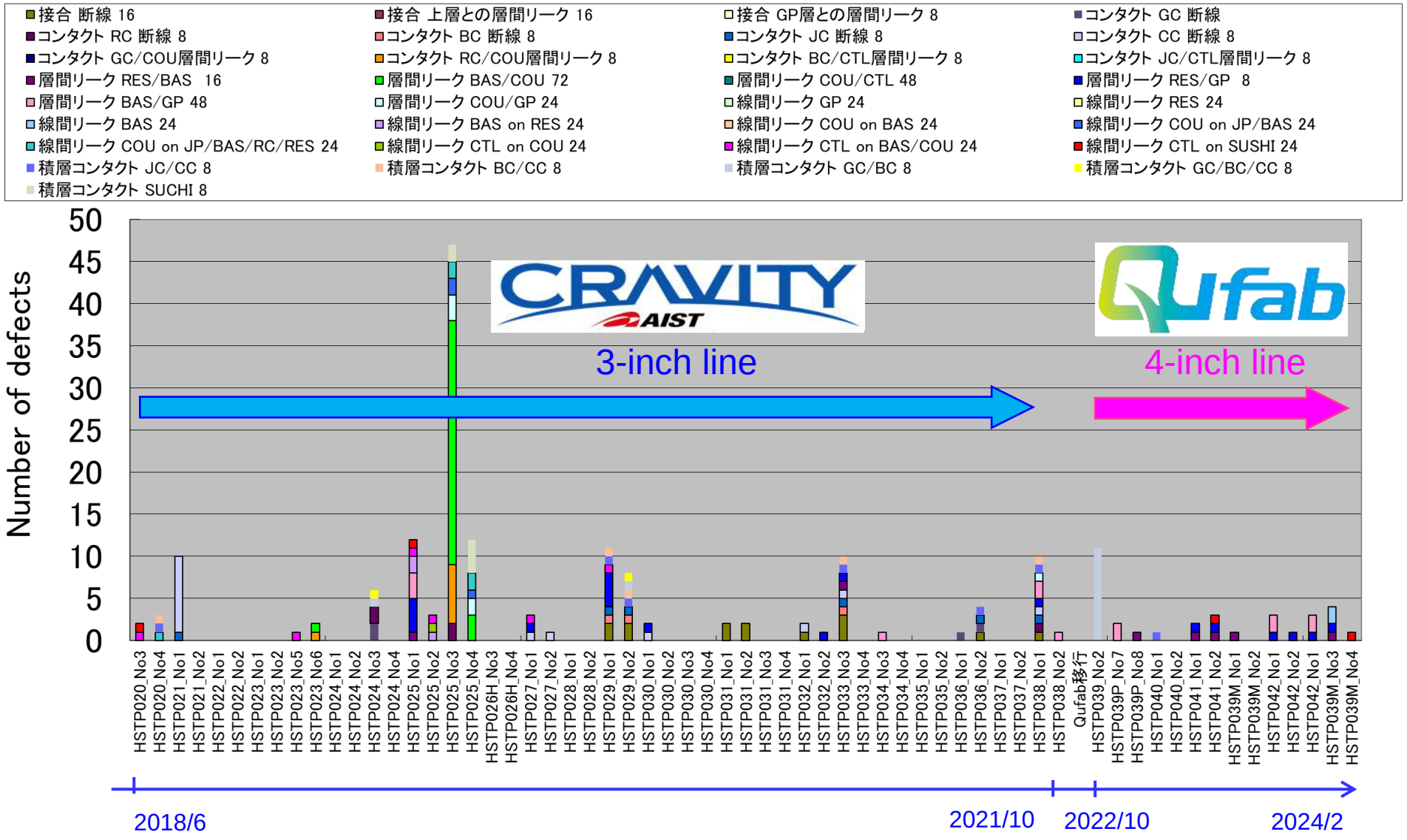
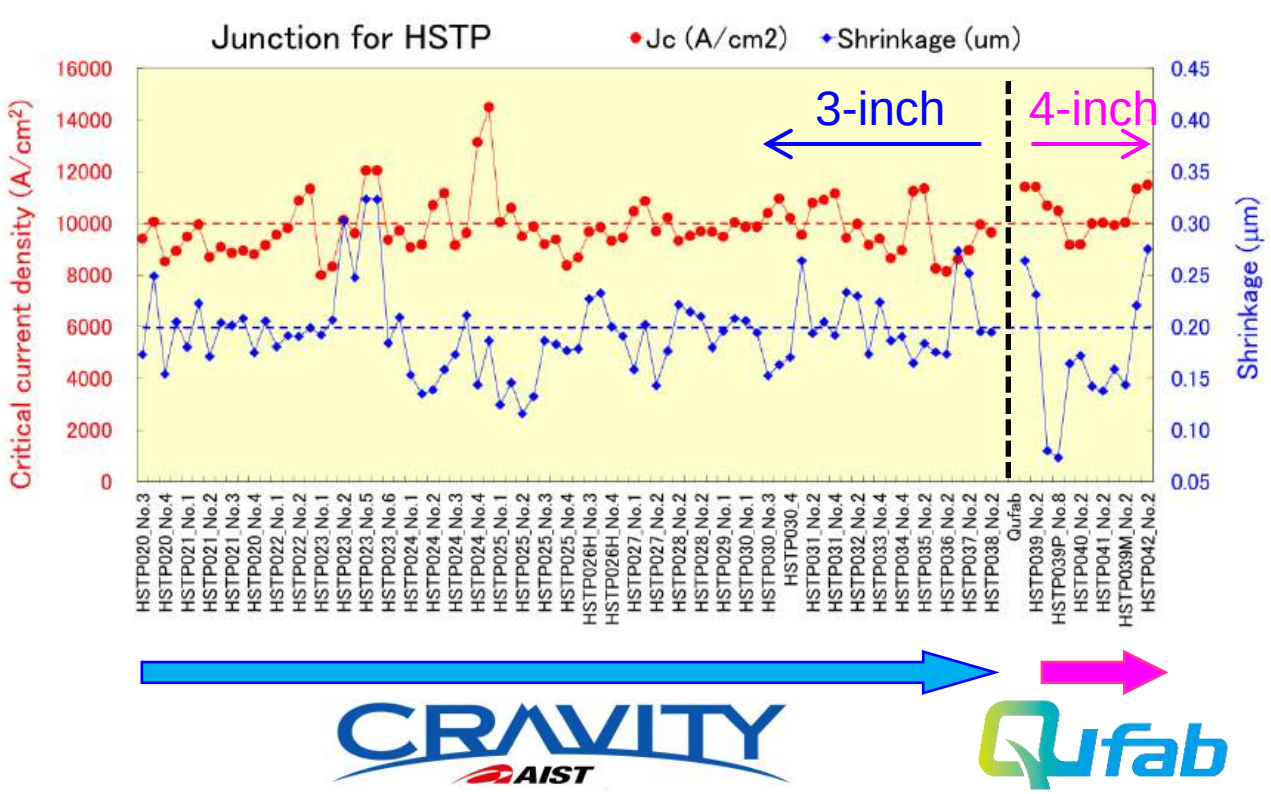
Changes in the number of HSTP process defects

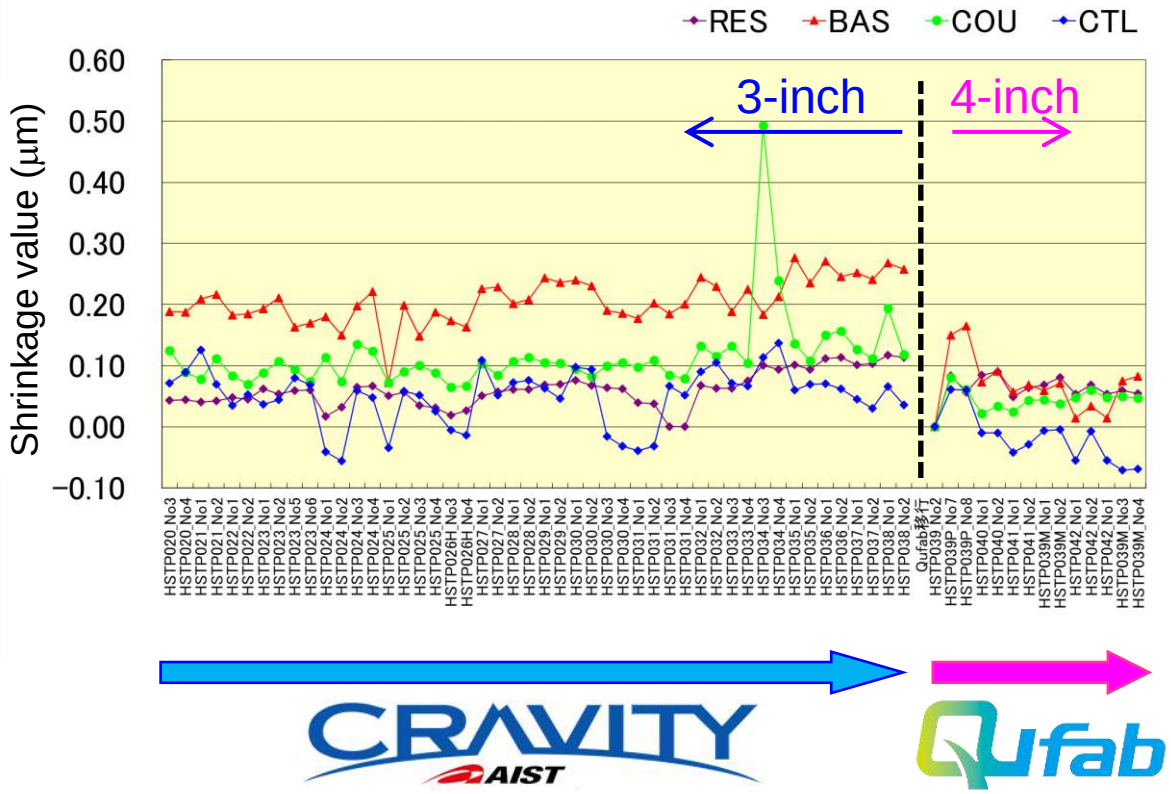


Parameter controllability of HSTP process (low-temperature measurement)

Changes in Jc and shrinkage value of JJ pattern



Changes in shrinkage value of wiring layers



Device structure of standard process for digital applications in Qufab

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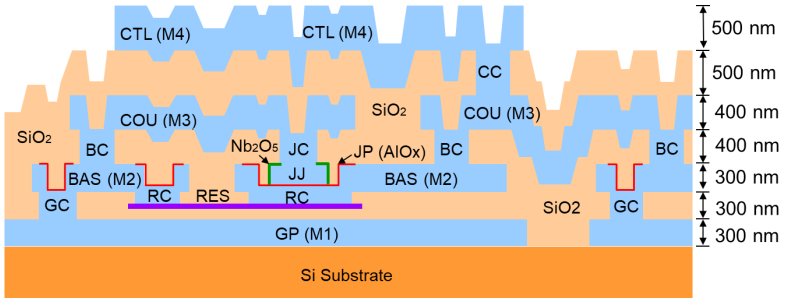
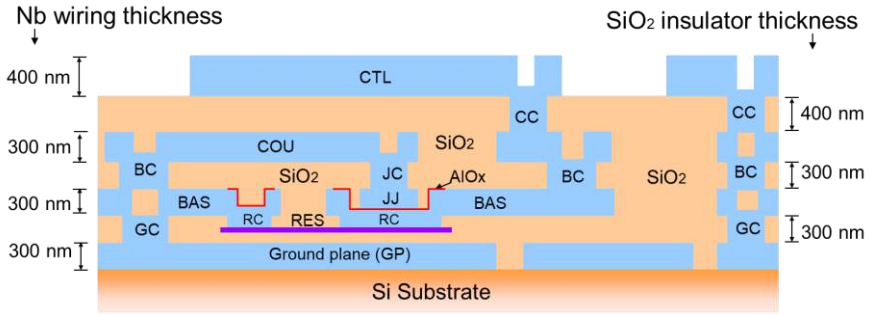
Nb 4-layers process



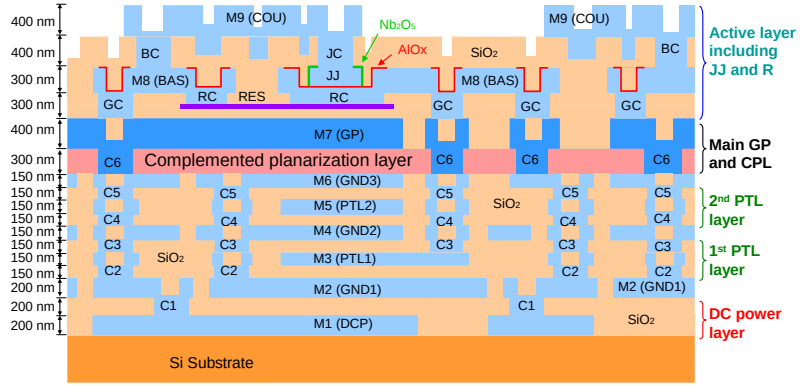
HSTP: J_c=10 kA/cm^2

Nb 4-layers process (fully planarized)

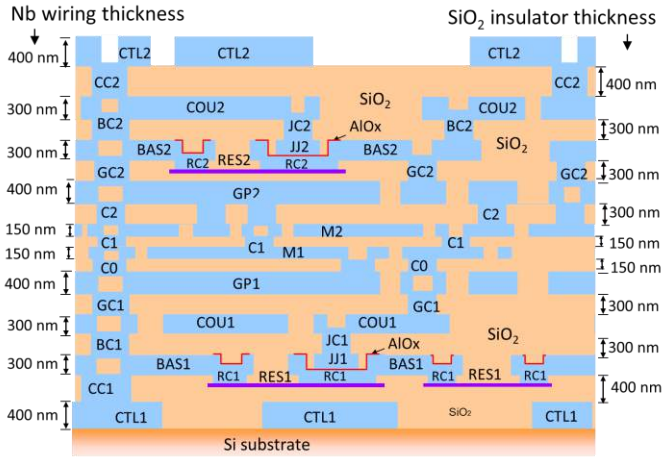


PHSTP: J_c=10 kA/cm^2
1KP: J_c=1 kA/cm^2

Advanced process



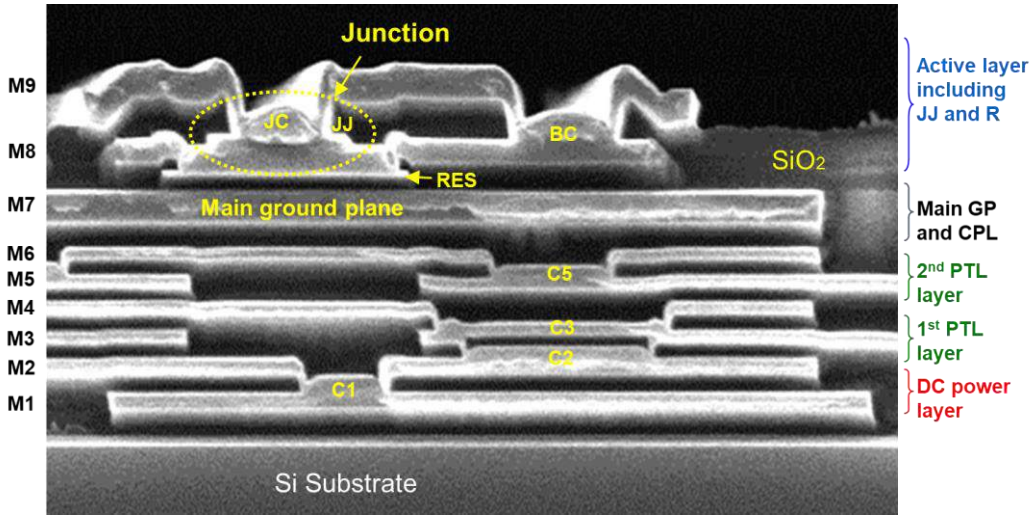
ADP2: Nb 9-layers, J_c=10 kA/cm^2



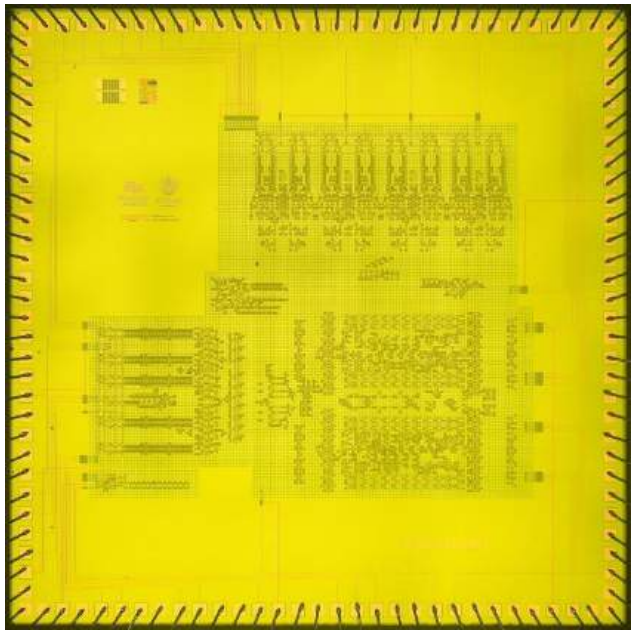
DGP: Nb 10-layers, J_c=10 kA/cm^2

Examples of digital circuit by advanced process

Nb 9-layers, ADP2 (partially planarized)



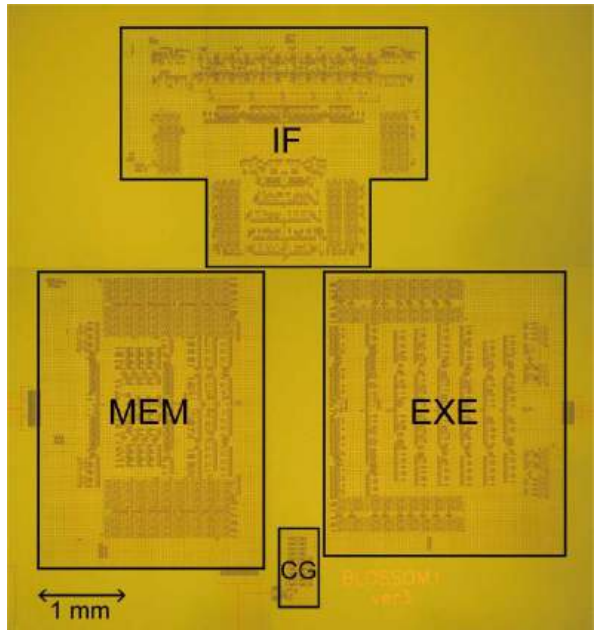
SFQ 4-bit parallel processor
Fabricated by AIST ADP2 process



Josephson junctions : 25,477
maximum frequency: 32 GHz

K. Ishida, et al., 2020 Symposia on VLSI Technology and Circuit

8-Bit general purpose processor
Fabricated by AIST ADP2 proces



Josephson junctions (JJs): 33,467
maximum frequency: 57.2 GHz

I. Nagaoka et al., *IEEE Asian Solid-State Circuits Conference*, Taipei, Nov. 2022.

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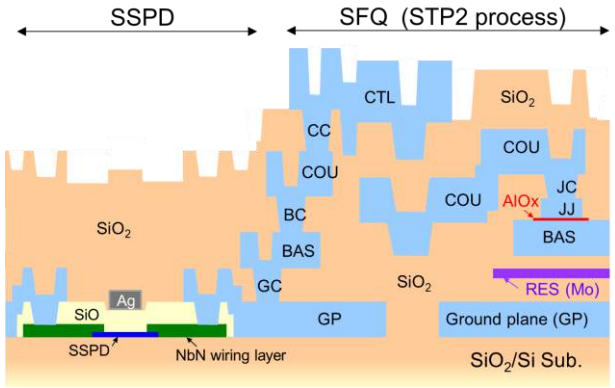
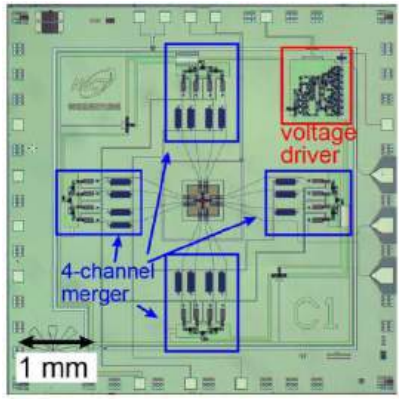
Application examples of superconducting digital circuits

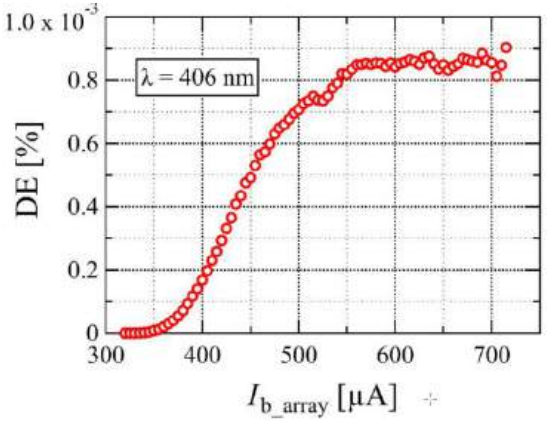
➢ SFQ signal processor for readout single-photon detector (SNSPD) arrays

- Monolithic integration process for SNSPD and SFQ circuit
- Multiplexing SNSPD arrays with high time resolution





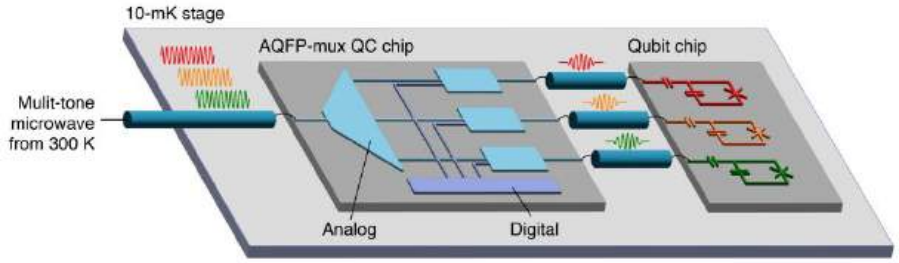
Measured detection efficiency curve

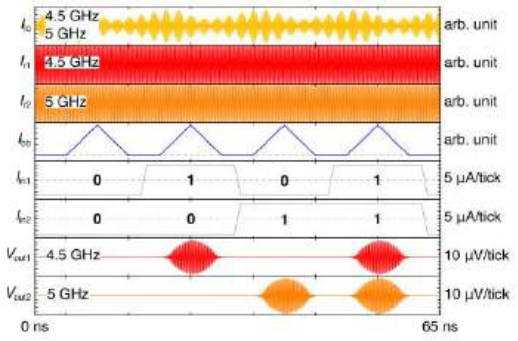


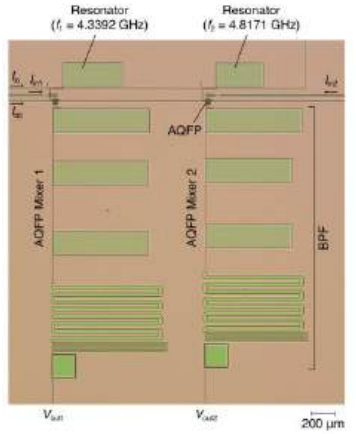
S. Miyajima et al, Appl. Phys. Lett. 122, 182602 (2023)

➢ Microwave-pulse generator using AQFP

- Aiming for signal processing at 10 mK using AQFP
- Ultra-low-power qubit control (81.8 pW per qubit)







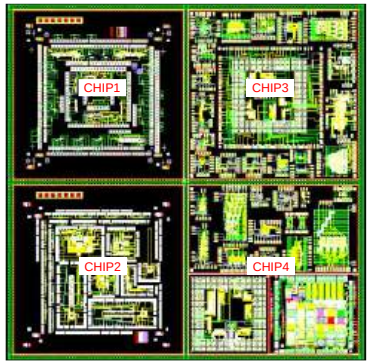
N. Takeuchi et al, NPJ Quantum Inf. 10, 53 (2024)

Outline

- Introduction of fabrication facility at AIST (Qufab)
- Superconducting digital circuits and their fabrication process
- Recent results at Qufab
- Qufab foundry service
- Summary

Qufab foundry service

Superconducting Quantum/digital Circuit Design (Users)

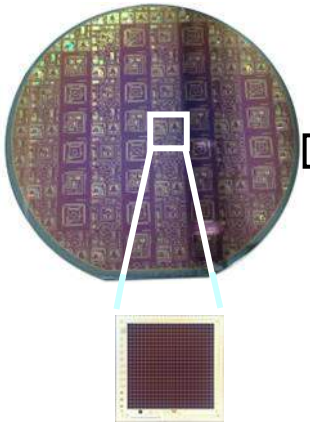


Qufab

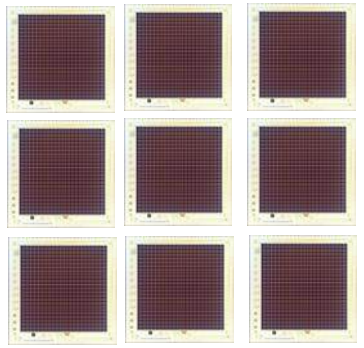
4-inchi Silicon wafer

Device and Circuit fabrication from 20-30 process equipment

Superconducting digital & quantum circuits



Deliver chips to the users

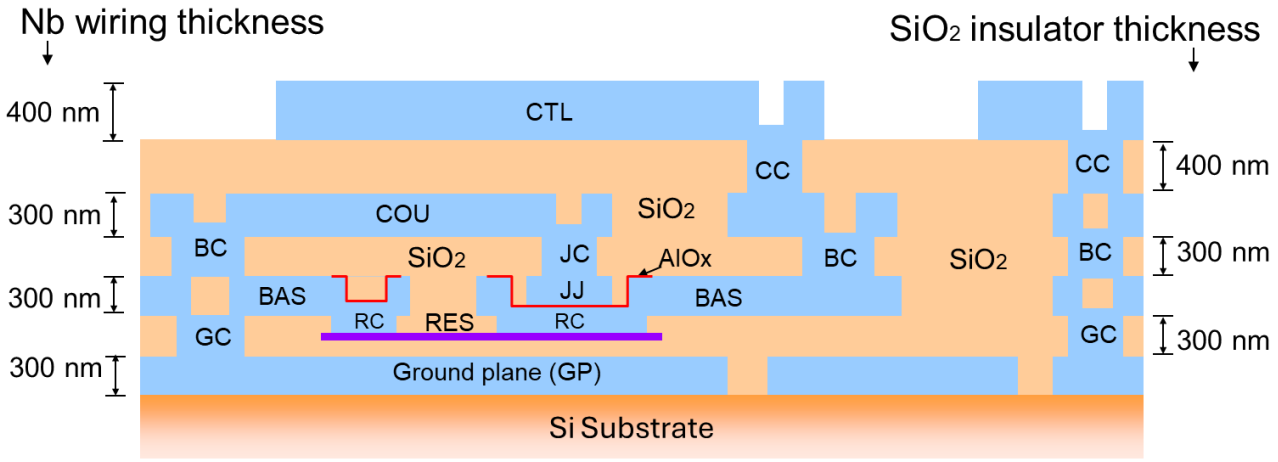


- Start : October 2024

  Qufab will stop between January to March in 2025 by several machine replacement
- Next application: Spring 2025
- Open to domestic and international users
- Open to public and private institutes
- Open to research and commercial use

Qufab foundry service

Fully planarized process, PHSTP



Nb: 4 layers
J_c: 10 kA/cm^2
$R_{\square}$: 2.4 Ω

Process TEG	Circuit TEG	A1	A2
A3	B1	C1	C2
C3	C4	C5	D1
D2	D3	E1	E2

One reticle

Chip size: 5 mm×5 mm
Reticle（22 mm×22 mm）：4×4 16 kinds of chip

About 14 chips fabricated for one kind in a 4-inch wafer

← Example: 5 institutes (A,B,C,D,E) share a reticle

Multiple users share one wafer

Summary

- AIST has developed fabrication process for superconducting integrated circuits and implemented many superconducting devices for long time.

- Qufab was started in 2022 as a renewal of CRAVITY,
  and we continue to develop superconducting digital circuit process and upgrade our equipment.
  (# of new equipment: 27 in 2023, >30 until March 2025)

- Our standard process, HSTP, is stable over a long period,
  and we also developed many advanced process for
  various purposes.

- Qufab started foundry service in October 2024.

G-QuAT
Quantum Device Research Team

Thank you for your kind attention.