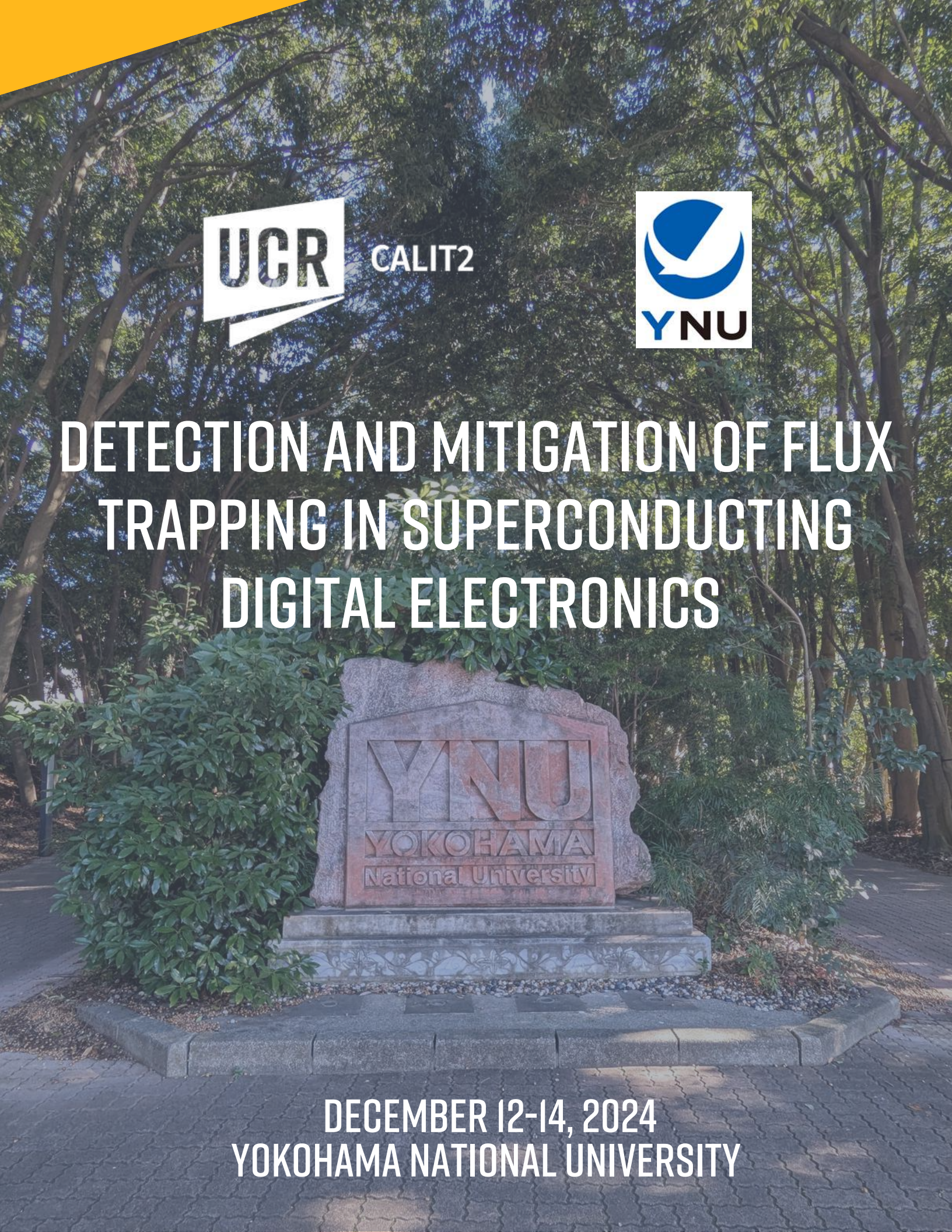


UCR CALIT2

YNU

DETECTION AND MITIGATION OF FLUX TRAPPING IN SUPERCONDUCTING DIGITAL ELECTRONICS

DECEMBER 12-14, 2024
YOKOHAMA NATIONAL UNIVERSITY

WORKSHOP DETAILS

Flux trapping remains a longstanding and unresolved challenge in the development of large-scale superconducting circuits. This workshop aims to foster in-depth discussions among researchers worldwide to explore methods for detecting and mitigating flux trapping in superconducting circuits. The workshop will be held in a hybrid format, offering both on-site and online participation options.

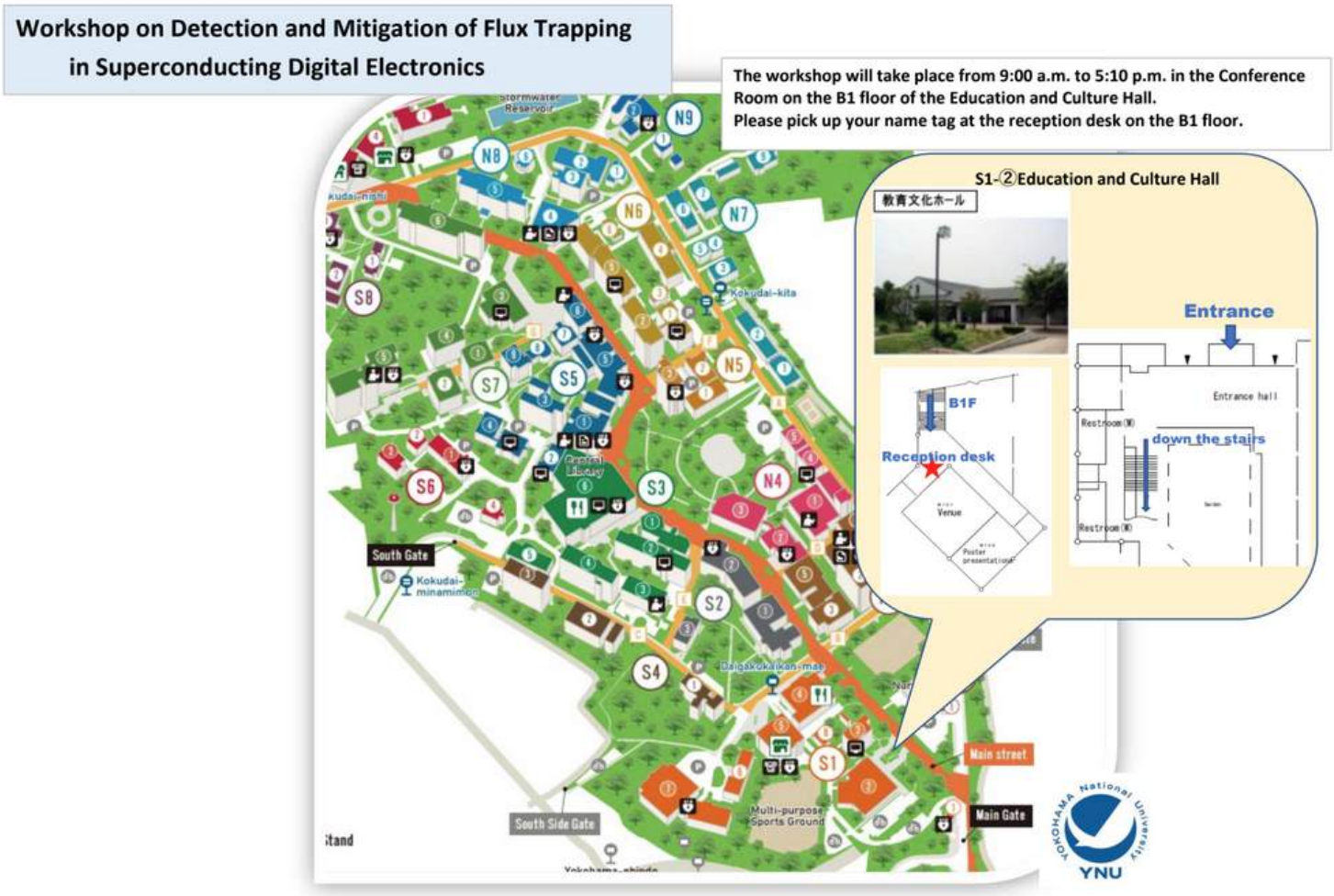
Dates and Time: Friday, December 13, 2024, 9:00 – 17:10 (JST)

Venue: Education and Culture Hall, Yokohama National University, Yokohama, Japan

Online link:
https://zoom.us/j/92289651469?pwd=brdFrW0JOLMSr2BGJztiNzlGisW6j4.1

UCR CALIT2 YNU IAS Institute of Advanced Sciences Yokohama National University

WORKSHOP LOCATION



Venue: Education and Culture Hall, Yokohama National University, Yokohama, Japan

Education and Culture Hall is indicated as S1-2 on the campus map:
https://www.ynu.ac.jp/english/about/access/map/

Access to the campus is explained here:
https://www.ynu.ac.jp/english/about/access/access/

Online link:
https://zoom.us/j/92289651469?pwd=brdFrW0JOLMSr2BGJztiNzlGisW6j4.1

AGENDA

SESSION DETAILS	
CHECK-IN **08:30 - 09:00**	
OPENING REMARKS **09:00 - 09:05** **Nobuyuki Yoshikawa,** Yokohama National University, JP	
High-Frequency Electrodynamics of Trapped Vortices in Superconductors **09:05 - 09:30** **Steven Anlage,** University of Maryland College Park, US	
Experimentally Detecting and Mitigating Trapped Flux at NIST **09:30 - 09:55** **Pete Hopkins,** National Institute of Standards and Technology (NIST), US	
Toward Trapped Flux Insensitive SFQ Logic Circuits **09:55 - 10:20** **Stephen Whiteley,** Synopsis Inc., US	
10:20 - 10:40	**COFFEE BREAK**
Superconducting Digital Circuits Fabrication Process at AIST **10:40 - 11:05** **Fumihiro China,** National Institute of Advanced Industrial Science and Technology (AIST), JP	
Recent Development of SFQ Circuits for milliKelvin Operation **11:05 - 11:30** **Masamitsu Tanaka,** Nagoya University, JP	

AGENDA

SESSION DETAILS	
Overview of large-scale AQFP efforts and FSDL plans at YNU **11:30 - 11:55** **Christopher Ayala,** Yokohama National University (YNU), JP	
Demonstration of Flux-bias-free Superconducting Flux Qubit with Ferromagnetic π-junction **11:55 AM - 12:20** **Taro Yamashita,** Tohoku University, JP	
12:20 - 13:30	**LUNCH**
Mitigation of Flux Trapping in Large-Format, Analog Low-Tc SQUID Arrays **13:30 - 13:55** **Kent Irwin,** Stanford University, US	
Optimizing Scanning SQUID Microscopy for Efficient Data Acquisition **13:55 - 14:20** **Kam Moler,** Stanford University, US	
Wide-field Quantitative Imaging of Superconducting Vortices Using Diamond Quantum Sensors **14:20 - 14:45** **Kento Sasaki,** University of Tokyo, JP	
14:45 - 15:45	**COFFEE BREAK & POSTER SESSION**
Research Activities on Superconducting Digital Electronics at NICT **15:45 - 16:10** **Hirotaka Terai,** National Institute of Information and Communications Technology (NICT), JP	

AGENDA

SESSION DETAILS
Benchmarking Stochastic Computing Neural Networks on Adiabatic Superconductor Devices **16:10 - 16:35** **Olivia Chen,** Kyushu University, JP
Low-critical-current AQFP/RSFQ Cell Library for Quantum and Stochastic Applications **16:35 - 17:00** **Naoki Takeuchi,** National Institute of Advanced Industrial Science and Technology (AIST), JP
CLOSING REMARKS **17:00 - 17:10** **Shane Cybart,** University of California Riverside, US

ABSTRACTS

ABSTRACT DETAILS

High-Frequency Electrodynamics of Trapped Vortices in Superconductors

Chung-Yang Wang, Jingnan Cai, Steven M. Anlage
Quantum Materials Center, Physics Department, University of Maryland College Park, US

We are interested in the microwave properties of individual (or few in number) magnetic vortices trapped in superconducting films. The objective is to understand how they respond to transient and steady-state exposure to microwave frequency currents, and how the pinning affects their response. The vortices are exposed to microwave frequency currents under controlled conditions through either a near-field magnetic microwave microscope [1], or through currents flowing in a co-planar waveguide transmission line. We study harmonic generation created when the trapped dc vortices are exposed to the rf currents, in part because this signal arises almost exclusively from the high-frequency response of the vortices. In particular we focus on second harmonic generation, and how this signal varies with temperature and location on the sample. The nonlinear response of trapped vortices is also calculated by means of time-dependent Ginzburg-Landau theory in COMSOL, which serves as a digital twin for the experiment [2]. The microwave microscope is modeled as an oscillating magnetic dipole that is held a few hundred nm above the surface of the superconductor. The second harmonic response of the vortices is calculated under many conditions, including location relative to the probe, type of pinning, temperature, and rf field/current amplitude. We also explore the properties of pinned vortices subjected to transient pulses, such as those they might experience in operating superconducting digital circuits. The status and future direction of this research program will be summarized.

[1] Chung-Yang Wang, Carlota Pereira, Stewart Leith, Guillaume Rosaz, Steven M. Anlage, "**Microscopic Examination of RF-cavity-quality Niobium Films through Local Nonlinear Microwave Response,**" Phys. Rev. Applied 22, 054010 (2024).
[2] Bakhrom Oripov and Steven M. Anlage, "**Time-dependent Ginzburg-Landau Treatment of RF Magnetic Vortices in Superconductors: Vortex-Semiloops in a Spatially Nonuniform Magnetic Field**," Phys. Rev. E 101, 033306 (2020).

ABSTRACTS

ABSTRACT DETAILS

Experimentally Detecting and Mitigating Trapped Flux at NIST

Pete Hopkins
National Institute of Standards and Technology (NIST), US

NIST has been developing superconducting circuits for primary voltage standards since the early 1970s and published its first experimental results on single-flux-quantum logic in 1993. Mitigation of trapped flux in these circuits has required careful circuit design and fabrication, cryostat design and construction, magnetic shielding, and measurement procedures. I will review the challenges and solutions we have developed in these areas. In addition, I will present experience we have in detecting trapped flux in our circuits and then share a particular circuit designed and simulated by Jackman and Fourie and measured at NIST to verify the flux trapping simulation models.

ABSTRACTS

ABSTRACT DETAILS

Toward Trapped Flux Insensitive SFQ Logic Circuits

Stephen Whitely
Synopsis Inc., US

When a metallic thin film is cooled below its superconducting transition temperature in the presence of a magnetic field, it can trap quantized bits of magnetic flux at apertures or defects within the film. These behave as tiny permanent magnets, which can alter the operation of nearby circuitry sensitive to magnetic fields. Unfortunately, this includes most circuits that use Josephson junctions, particularly those where superconducting loops containing Josephson junctions and inductors appear, which includes most if not all known logic and memory circuits. To operate such circuits, mitigation strategies must be employed, which include careful use of magnetic shielding in-place during cooldown, and placement of artificial trapping centers ("moats") to preferentially trap any flux away from sensitive locations. Being a stochastic process implies that it may not be possible to completely eliminate trapped flux, and this may be an increasing problem as circuits become more dense, yet more complex and larger physically. Another mitigation approach may be to develop circuits that are less sensitive to magnetic fields. Here, we propose a single flux quantum (SFQ) library of digital gates and flops engineered to reduce sensitivity to magnetic flux by use of kinetic inductance of Josephson junctions replacing geometric inductors. This substantially reduces the field sensitivity, as only residual parasitic geometric inductance couples to the external magnetic field. Use of this principle, among others mentioned, may represent good progress in trapped flux mitigation for these circuits. However, if transformers are needed, geometric inductance will be required in these devices so the principle will not be applicable there.

ABSTRACTS

ABSTRACT DETAILS

Superconducting Digital Circuits Fabrication Process at AIST

Fumihiro China, Shuichi Nagasawa, Mutsuo Hidaka, Fuminori Hirayama, Koh-ichi Nittoh, and Go Fujii
National Institute of Advanced Industrial Science and Technology (AIST), JP

When a metallic thin film is cooled below its superconducting transition temperature in the presence of a magnetic field, it can trap quantized bits of magnetic flux at apertures or defects within the film. These behave as tiny permanent magnets, which can alter the operation of nearby circuitry sensitive to magnetic fields. Unfortunately, this includes most circuits that use Josephson junctions, particularly those where superconducting loops containing Josephson junctions and inductors appear, which includes most if not all known logic and memory circuits. To operate such circuits, mitigation strategies must be employed, which include careful use of magnetic shielding in-place during cooldown, and placement of artificial trapping centers ("moats") to preferentially trap any flux away from sensitive locations. Being a stochastic process implies that it may not be possible to completely eliminate trapped flux, and this may be an increasing problem as circuits become more dense, yet more complex and larger physically. Another mitigation approach may be to develop circuits that are less sensitive to magnetic fields. Here, we propose a single flux quantum (SFQ) library of digital gates and flops engineered to reduce sensitivity to magnetic flux by use of kinetic inductance of Josephson junctions replacing geometric inductors. This substantially reduces the field sensitivity, as only residual parasitic geometric inductance couples to the external magnetic field. Use of this principle, among others mentioned, may represent good progress in trapped flux mitigation for these circuits. However, if transformers are needed, geometric inductance will be required in these devices so the principle will not be applicable there.

ABSTRACTS

ABSTRACT DETAILS

Recent Development of SFQ Circuits for milliKelvin Operation

Masamitsu Tanaka
Nagoya University, JP

In this talk, the recent development of a low-power SFQ standard cell library aiming at operation with superconductors will be presented. The circuits were fabricated using the 250 A/cm² process and low-voltage design, resulting in the power consumption of 1/50 or 1/250 of the conventional SFQ circuits operating at 4.2 K. The topic will include mask layout design, measurement using cryocoolers, and experimental results at 300 mK or below.

Overview of large-scale AQFP efforts and FSDL plans at Yokohama National University

Christopher Ayala
Institute of Advanced Sciences, Yokohama National University, JP, Atlantic Quantum, US

Adiabatic quantum-flux-parametron (AQFP) logic can operate below 50 *KT* at 5 GHz, which makes it attractive for energy-efficient computing systems needed in today's information-based society. At Yokohama National University (YNU), we have been striving to develop AQFP logic and superconductor digital electronics in general towards practical applications. In this talk, we highlight some of the efforts at YNU towards large-scale design of AQFP circuits including clocking networks, sequential design approaches, and demonstration of complex circuits such as SHA-3 permutation units. We will also outline our recent progress and plans for the DEVCOM/LPS supported Foundations of Superconducting Digital Logic (FSDL) including our flux trapping investigations using the AIST Qufab foundry in Japan as well as MIT Lincoln Laboratory's SFQ5ee process, and investigating circuit design approaches amiable to leveraging circuit edit techniques via focused helium ion beam lithography.

ABSTRACTS

ABSTRACT DETAILS

Demonstration of Flux-bias-free Superconducting Flux Qubit with Ferromagnetic π-junction

Taro Yamashita, Sunmi Kim, Leonid V. Abdurakhimov, Duong Pham, Wei Qiu, Hirotaka Terai, Sahel Ashhab, Shiro Saito, Kouichi Semba
Tohoku Univ., Nagoya Univ., National Institute of Information and Communications Technology, NTT Corporation, IQM Finland Oy, The University of Tokyo

Conventional superconducting flux qubits require half-flux-quantum bias through the qubit loop, which complicates the on-chip integration. It has been proposed that by inducing a π-phase shift in the superconducting order parameter using a superconductor/ferromagnet/superconductor Josephson junction (π-junction), it is possible to realize a flux qubit operating at zero magnetic flux. Here, we report the demonstration of flux-bias-free flux qubit based on three NbN/AlN/NbN Josephson junctions and a NbN/PdNi/NbN ferromagnetic π-junction [1]. The qubit lifetime is in the microsecond range, which will be limited by quasiparticle excitations in the metallic ferromagnet layer. Our results pave the way for developing quantum coherent devices, including qubits and sensors, that utilize the interplay between ferromagnetism and superconductivity.

[1] S. Kim et al., Communications Materials volume 5, Article number: 216 (2024).
This work was partly supported by JST CREST (Grant No.JPMJCR1775), JSPS KAKENHI (JP19H05615),JST ERATO (JPMJER1601), MEXT Quantum Leap Flagship Programs (JPMXS0120319794 and JPMXS0118068682).

ABSTRACTS

ABSTRACT DETAILS

Mitigation of Flux Trapping in Large-Format, Analog Low-Tc SQUID Arrays

Kent Irwin
Stanford University, US

NA

Optimizing Scanning SQUID Microscopy for Efficient Data Acquisition

Kam Moler
Stanford University, US

Scanning SQUID Microscopy is a powerful technique for imaging magnetic fields, magnetic susceptibility, and current flow with high sensitivity. This presentation will discuss key considerations for acquiring meaningful data from SQUID microscopy images of superconducting circuits, including optimizing scan parameters, understanding noise sources, and interpreting image features. We will also explore strategies for increasing sample throughput.

ABSTRACTS

ABSTRACT DETAILS

Wide-field Quantitative Imaging of Superconducting Vortices Using Diamond Quantum Sensors

Kento Sasaki
University of Tokyo, JP

We are developing magnetometry using nitrogen-vacancy (NV) centers in diamonds as quantum sensors to explore solid-state physics. By using diamond chips that contain NV center ensembles only near the surface, it is possible to perform quantitative imaging of the stray magnetic field from magnetic and superconducting materials over a wide field of view. In this presentation, we explain the principle of our technique and show recent results on quantum vortices in cuprate superconductors.

Research Activities on Superconducting Digital Electronics at NICT

Hirotaka Terai, Shigeyuki Miyajima, Shigehito Miki
Advanced ICT Research Institute, National Institute of Information and Communications Technology (NICT), JP

We have developed cryogenic signal processors based on single-flux-quantum circuits for multi-pixel SNSPD arrays.To realize a multi-pixel SNSPD system that operates in a 0.1W GM cryocooler together with an SFQ signal processor, it is important to suppress the joule heating associated with the dc power supply to the SFQ circuits. In this talk, we introduce our research activities focusing on the implementation of SFQ circuits in a compact GM cryocooler.

ABSTRACTS

ABSTRACT DETAILS

Benchmarking Stochastic Computing Neural Networks on Adiabatic Superconductor Devices

Olivia Chen
Kyushu University, JP

Stochastic computing (SC), a paradigm that represents and processes data using randomized bit-streams, offers substantial reductions in hardware complexity and improved tolerance to errors—an appealing trait for emerging technologies and noise-resilient applications [Gaines, B. R. (1969). _Stochastic Computing Systems_. In: Advances in Information Systems Science, Vol. 2, pp. 37–172, Springer]. In this work, we integrate an SC-based framework with Adiabatic Quantum-Flux-Parametron (AQFP) superconducting logic—a highly energy-efficient superconducting logic family [Takeuchi, Y., et al. (2014). _IEEE Trans. Appl. Supercond._, 24(3), 1–7]—and use empirical data modeling to apply these techniques to mainstream neural network workloads [Krizhevsky, A., et al. (2017). _Commun. ACM_, 60(6), 84–90]. Our analysis provides insights into the performance and potential advantages of SC-based AQFP implementations in achieving efficient, error-tolerant neural network processing.

Low-critical-current AQFP/RSFQ Cell library for Quantum and Stochastic applications

Naoki Takeuchi[1], Taiki Yamae[1], Yuki Hironaka[2], Shuichi Nagasawa[1], Yuki Yamanashi[2], and Nobuyuki Yoshikawa[2]
[1]National Institute of Advanced Industrial Science and Technology (AIST), [2]Yokohama National University, JP

Superconductor logic families, such as AQFP and RSFQ logic, operate with low power dissipation and high operating frequencies, thus having a potential to be used in various applications. In this study, we report low-critical-current AQFP and RSFQ cell libraries, dedicated to the design of quantum and stochastic systems. The cell libraries enable qubit interface circuits to operate with very small power dissipation at ~10 mK and stochastic electronics to easily induce stochastic operations. We demonstrate basic low-critical-current AQFP and RSFQ logic cells at 4.2 K.

PRESENTATIONS

PRESENTATIONS DETAILS
Superconducting Circuit Edit: Capabilities at UCR **Jay LeFebvre,** University of California Riverside (UCR), US
Simulating Adiabatic Digital Logic in High Tc Superconductors **Joseph Barrera,** UCR, US
Study of Stochastic Signal Processing Circuits Using Single Flux Quantum Circuits **Kaito Asaka,** Yokohama National University, JP
Hardware Implementation of Scalable Bayesian Networks Using Single Flux Quantum Circuits **Rikuo Yamanaka,** Yokohama National University, JP
Design of Adiabatic Quantum-Flux-Parametron Using Double Gate Process **Aki Nagai,** Yokohama National University, JP
Investigation of the Phase Sensitivity of a Josephson Parametric Oscillator at Cryogenic Temperatures **Itaru Machimura,** Yokohama National University, JP
Multithreading of the Adiabatic Quantum Flux Parametron Data Path **Yuto Omori,** Yokohama National University, JP
Design and Performance Evaluation of a Double-switching TFF using Single-Flux-Quantum Circuits **Riko Tasaki,** Yokohama National University, JP

POSTERS

POSTER DETAILS
Research on a Direct-Quantum-Flux-Parametron Circuit Using Dual-rail Logic **Yuta Hasegawa,** Yokohama National University, JP
Small-Area Arithmetic Circuits Based on Unary Coding for Single Flux Quantum Circuits **Zeyu Han,** Yokohama National University, JP
Design of Superconducting Stochastic Adder Circuit Without Multiplexer **Yuya Mandai,** Yokohama National University, JP
Development of High-Speed and Versatile Circuit Parameter Optimization Tool for Superconductor **Sho Matsuoka,** Yokohama National University, JP
Design of circuits to test the effects of radiation on SFQ circuits **Kazuto Osakabe,** Yokohama National University, JP