National Institute of Standards and Technology
U.S. Department of Commerce

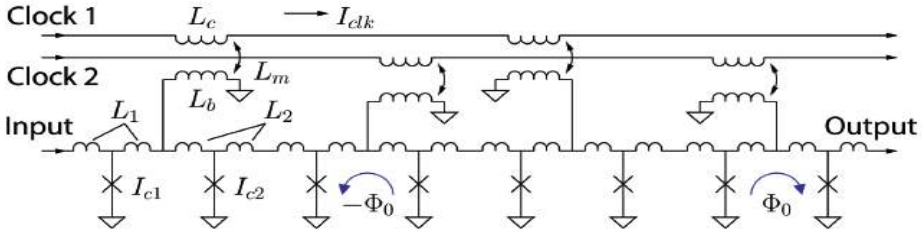
Experimentally detecting and mitigating trapped flux at NIST

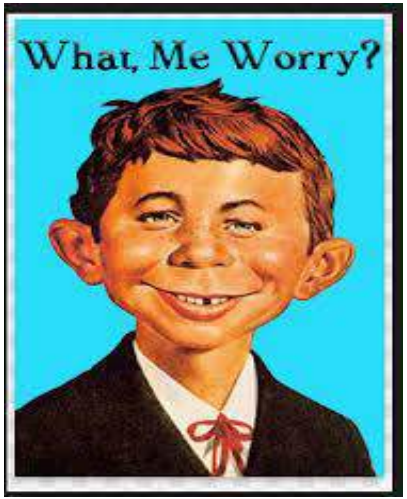
Presenter: Pete Hopkins
Superconductive Electronics Group

Superconductive Electronics Group

Why is trapped flux bad for SFQ logic?

SFQ Circuits are based on Single Flux Quanta signals





Trapped flux are one or more single flux quanta

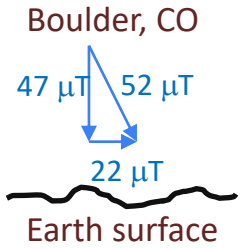
Fluxons trapped in circuits produce lower operating margins and/or nonfunctional circuits.

- Phase shift in JJs and SQUIDs
- Alters the bias of circuits

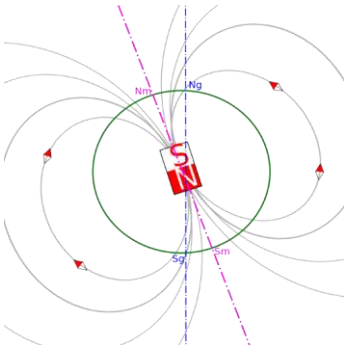
Magnitude and direction of Earth's field

http://en.wikipedia.org/wiki/Earth's_magnetic_field

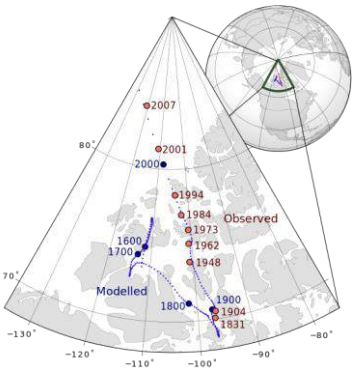
1. Source: geodynamo -> motion of molten iron alloys in outer core
2. Acts to deflect Solar Wind (charged particles that would carry away the Ozone, etc.)
3. Magnitude: 25-65 μT surface (highest near the poles, lowest near equator)
   - ~52 μT (Boulder) http://upload.wikimedia.org/wikipedia/commons/c/c7/WMM2010_F_MERC.pdf
4. Direction: Straight down/up at N/S poles, horizontal at equator
   - ~65 degrees inclination (surface), ~10 deg declination (NEast) at Boulder
   - http://en.wikipedia.org/wiki/File:World_Magnetic_Inclination_2010.pdf
   - http://en.wikipedia.org/wiki/File:World_Magnetic_Declination_2010.pdf
5. Reverses at irregular intervals, averaging several x 100k years
6. N & S poles wander independently; not directly opposite



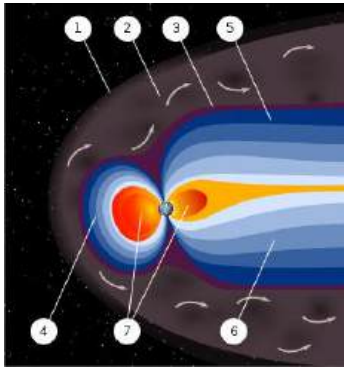
Dipole Approximation



Movement of N pole vs year



Magnetosphere



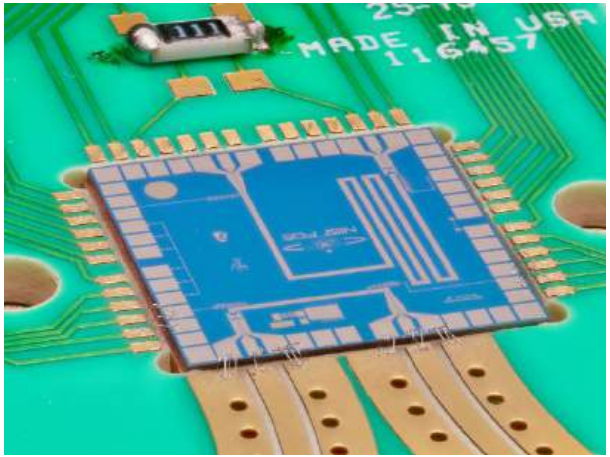
Outline

General guidelines

1. Best practices from previous US digital programs
2. Literature list
3. Simulation/measurement example from SuperTools

NIST-specific practices

1. Circuit design
2. Simulation
3. Fabrication
4. Cryostat design and shielding
5. Measurement protocols



Best practices from US digital programs (2016)

Q: What level of (perp.) magnetic flux density ***B*** can we tolerate at chip level?

Answer: Must have no trapped flux within circuits

Practical Answer: Mitigation strategies

1. **Reduce ambient field at chip by 100X** (from ~50 μT field to ~500 nT).
   - Passive mu-metal shielding or passive + active field cancellation

2. **Cell design strategy: 1 trapped flux quantum per moat (max)**
   - For 500 nT: 1 flux quantum per 64 μm x 64 μm cell size
   - 2-4 border moats per unit cell, moat size follows simple design rules
   - Option: ground plane wire lattice

3. **Holistic FAB approach for the full 8 or 10-metal layer stack**

   Engineer the master ground plane: T_c and vortex freezing/pinning temp T_f.
   - Highest T_c and T_f by > ~ 0.1 K
   - Low density of unintentional pinning centers (large $\Delta T = T_c - T_f$ value).
   - Not used for carrying high currents (which generate magnetic fields).
   - Moat alignment /2nd ground plane strategy

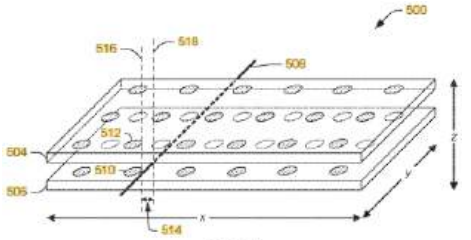


FIG. 5

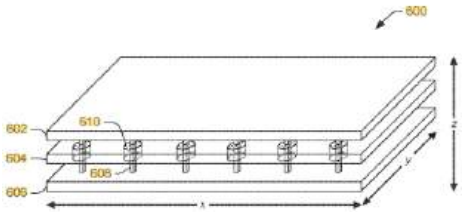


FIG. 6

US Patent: US20200287118A1
Northrop Grumman, 2022

A. Herr et al.

https://patents.google.com/patent/US20200287118A1/en

Best practices from US digital programs (2016)

Q: What level of magnetic flux density ***B*** can we tolerate at chip level?

Answer: Must have no trapped flux within circuits

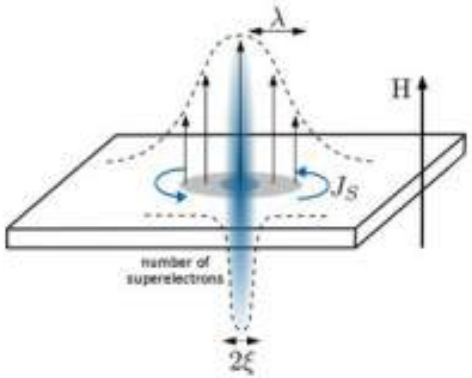
Practical Answer: Mitigation strategies

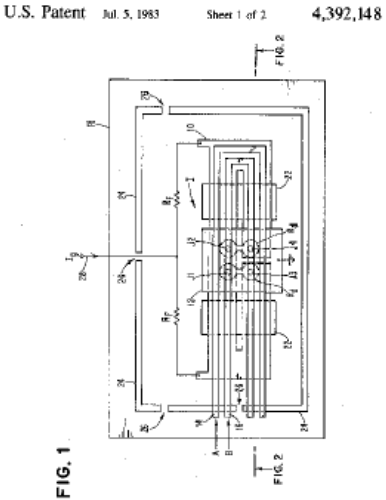
4. “Move” the flux quanta before they freeze in place

- e.g. use moats or segmented ground planes
- Cool slowly through T_c (~ 1 mK/s)

5. Add no additional field when $T < T_c$

- Avoid high current densities, etc.
- Multiple thermal cycles to verify performance (min of 3)





US4392148 A Patent
IBM, 1983
Wen H. Chang et al.

Best practices from US digital programs (2016)

Q: Do we need better design tools, supporting data, and procedures for mitigating flux trapping?

A: Yes! Design tools are non-existent; moat design immature; measurement procedures are empirical

Practical Answer

1. **Need simulation EDA tools: This could be part of SuperTools.**
   - Jackman and Fourie 2016 IEEE Trans. Appl. Supercond. 26 1–5

2. **Need model-to-hardware correlation to evaluate moat geometry, size, placement, #, etc.**
   - Fourie and Jackman publications (2016-)
   - Circuits with large input currents? speculate that these require unique moat designs.

3. **Measurement procedures are empirical**
   - Cool slowly through T_c (~ 1-10 mK/s)
   - Limiting current on bias lines for circuits requiring large input currents

Flux Trapping Literature

Reviews:

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2. Tinkham, M.: *Introduction to Superconductivity* (2nd ed.), Dover, NY (1996)
3. Van Duzer, T. and Turner, C.W.: *Principles of Superconducting Devices and Circuits* (2nd Ed.), Prentice Hall, NJ (1999)

Technical Papers

1. Wen H. Chang, Tushar R. Gheewala, Erik P. Harris, US4392148 A awarded to IBM, 1983 (Moat Patent)
2. G. Stan, S. B. Field, and J. M. Martinis, “Critical Field for Complete Vortex Expulsion from Narrow Superconducting Strips,” *Physical Review Letters*, vol. 92, no. 9, p. 097003, Mar. 2004. http://link.aps.org/doi/10.1103/PhysRevLett.92.097003
3. Y. Polyakov, S. . Narayana, and V. K. Semenov, “Flux Trapping in Superconducting Circuits,” *IEEE Transactions on Applied Superconductivity*, vol. 17, no. 2, pp. 520–525, 2007. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=4277667
4. M. Jeffery, T. Van Duzer, J. R. Kirtley, and M. B. Ketchen, “Magnetic imaging of moat-guarded superconducting electronic circuits,” *Applied Physics Letters*, vol. 67, no. 12, p. 1769, 1995.
5. Q. P. Herr, J. Osborne, M. J. A. Stoutimore, H. Hearne, R. Selig, J. Vogel, E. Min, V. V. Talanov, and A. Y. Herr, “Reproducible operating margins on a 72 800-device digital superconducting chip,” *Superconductor Science and Technology*, vol. 28, no. 12, p. 124003, Dec. 2015.
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7. D. Gaidarenko, R. Robertazzi, “High Performance Packaging System for Superconducting Electronics,” *IEEE Transactions on Applied Superconductivity,”* vol. 9, no. 2, 3668-3671 (1999)
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9. S. Narayana, “Large Scale Integration Issues in Superconducting Circuits,” Ph.D., Stony Brook University, 2010. http://hdl.handle.net/1951/55560
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11. Ter Harr, I.D.: *Men of Physics: L. D. Landau*, Oxford:Pergamon (1965)

Flux Trapping Literature

12. S. Narayana, Y. A. Polyakov, and V. K. Semenov, “Evaluation of Flux Trapping in Superconducting Circuits,” *IEEE Transactions on Applied Superconductivity*, vol. 19, no. 3, pp. 640–643, Jun. 2009. DOI: 10.1109/TASC.2009.2018248
13. V. K. Semenov, Y. A. Polyakov, and S. K. Tolpygo, “New AC-Powered SFQ Digital Circuits,” *IEEE Transactions on Applied Superconductivity*, vol. 25, no. 3, pp. 1–7, Jun. 2015. DOI: 10.1109/TASC.2014.2382665
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    R. P. Robertazzi, I. Siddiqi and O. Mukhanov, "Flux trapping experiments in single flux quantum shift registers," in *IEEE Transactions on Applied Superconductivity*, vol. 7, no. 2, pp. 3164-3167, June 1997. DOI: 10.1109/77.622002
15. F. Furuta *et al*., "New logic circuits based on SFQ signals," in *IEEE Transactions on Applied Superconductivity*, vol. 9, no. 2, pp. 3553-3556, June 1999. DOI: 10.1109/77.783797
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18. Bjoern Ebert, Torsten Reich, Thomas Ortlepp, Pascal Febvre, F. Hermann Uhlmann, "Influence of trapped flux on critical currents of Josephson junctions," IEICE Electronics Express, Vol. 5 (2008) No. 11 P 431-436, DOI: 10.1587/elex.5.431
19. K. Jackman and C. J. Fourie, "Flux Trapping Analysis in Superconducting Circuits," *IEEE Transactions on Applied Superconductivity*, vol. 27, no. 4, pp. 1-5, June 2017, Art no. 1300105, doi: 10.1109/TASC.2016.2642590.
20. C. J. Fourie and K. Jackman, "Experimental Verification of Moat Design and Flux Trapping Analysis," *IEEE Transactions on Applied Superconductivity*, vol. 31, no. 5, pp. 1-7, Aug. 2021, Art no. 1300507, doi: 10.1109/TASC.2021.3051582.
21. Coenrad J Fourie et al., ”Evaluation of flux trapping moat position on AQFP cell performance,” J. Phys.: Conf. Ser. 1975 012027, 2021 doi 10.1088/1742-6596/1975/1/012027
22. Anna. Y. Herr et al, “Superconductor ground plane patterning geometries that attract magnetic flux,” US Patent: US20200287118A1 (2022) https://patents.google.com/patent/US20200287118A1/en
23. Y. A. Polyakov, V. K. Semenov and S. K. Tolpygo, “3D Active Demagnetization of Cold Magnetic Shields,” *IEEE Trans. Appl. Supercond.*, vol. 21, pp. 724-727, June 2011. DOI: 10.1109/TASC.2010.2091384

Critical field in superconducting Nb strips

G. Stan, S. B. Field, and J. M. Martinis, "Critical Field for Complete Vortex Expulsion from Narrow Superconducting Strips," *Physical Review Letters*, vol. 92, no. 9, p. 097003 Mar 2004 http://link.aps.org/doi/10.1103/PhysRevLett.92.097003

Opposing forces: Image force (expel flux) vs. Flux/Meisner currents (push flux to center)

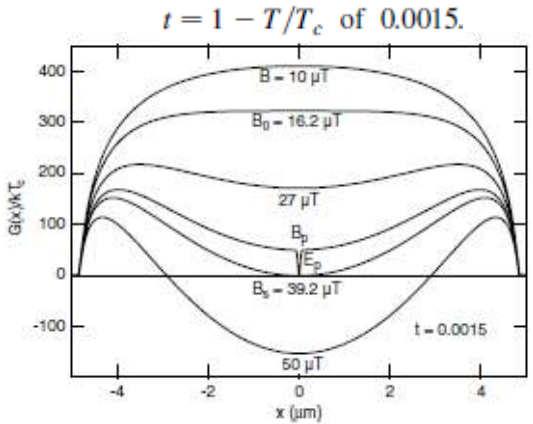
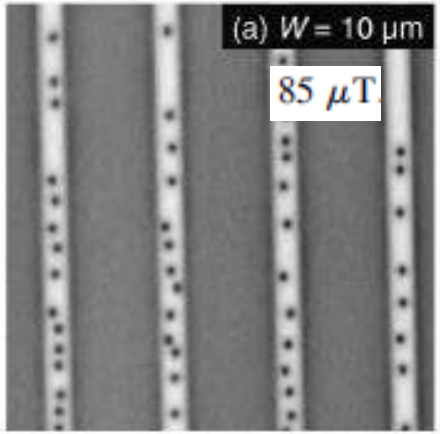
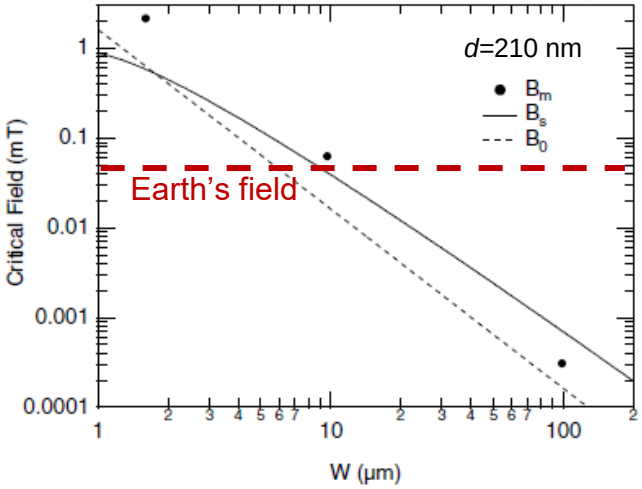


FIG. 1. The Gibbs free energy (Ref. [2]) of a single vortex located at position x at several values of the applied field B, at a reduced temperature $t = 1 - T/T_c$ of 0.0015. The curve at $B_p = 36\ \mu$T includes schematically a pinning well of depth $E_p \approx 50\, kT_c$.



$$B_m \approx \Phi_0/W^2.$$

For in-plane Λ >> W $\quad \Lambda = 2\lambda^2/d$

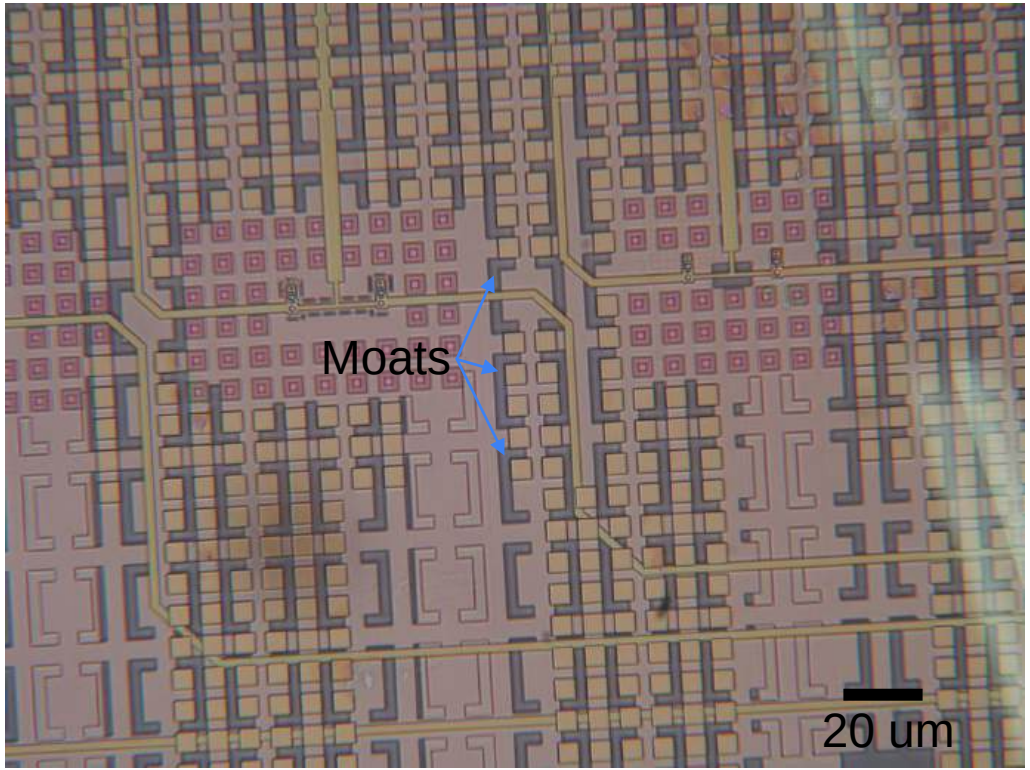


Conclusions:

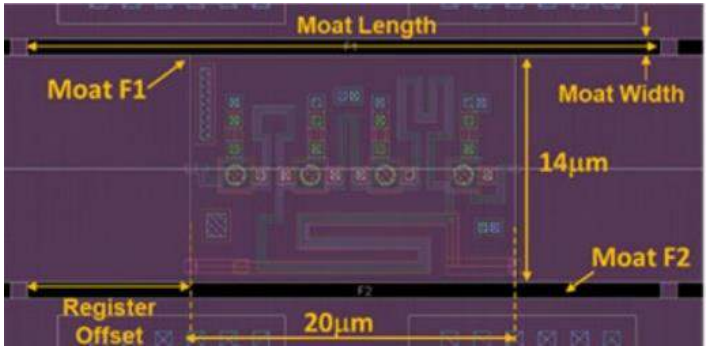
Universal: Independent of SC materials parameters (if $\Lambda(T_f)$ >> W)

Design: use narrow wires, avoid large ground planes if possible

Examples of moat designs



Moats divide GP into 14 um strips



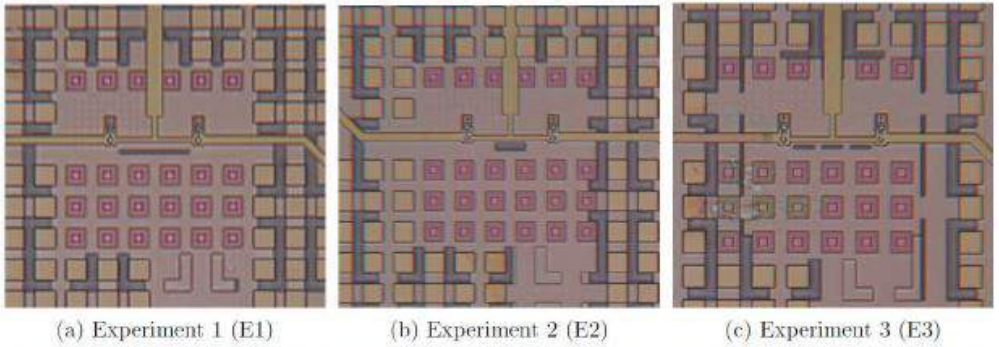
Meninger and Tolpygo (2024)
https://arxiv.org/pdf/2411.02749

C. J. Fourie et al., *IEEE TAS (2021)* doi: 10.1109/TASC.2021.3051582.

Slide from Coenrad Fourie, ASC 2020

Under IARPA SuperTools programme (ColdFlux project), we designed a set of flux linkage experiments[3].

- Design: SU Fab: MIT-LL Test: NIST



(a) Experiment 1 (E1) (b) Experiment 2 (E2) (c) Experiment 3 (E3)

(d) Experiment 4 (E4) (e) Experiment 5 (E5) (f) Experiment 6 (E6)

Figure: SQUID test structures

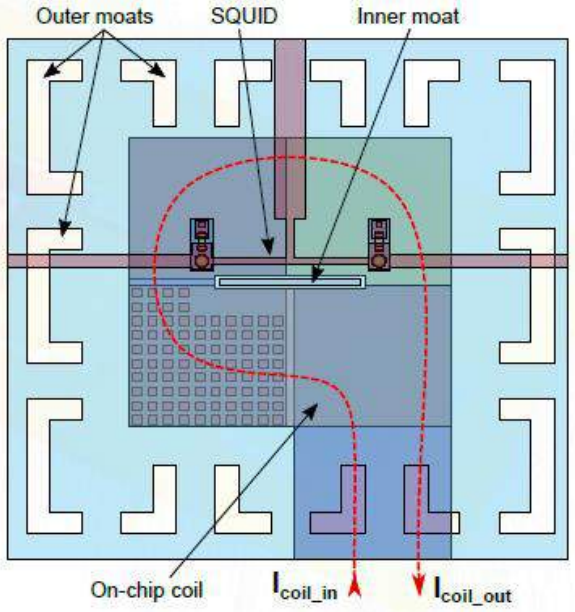
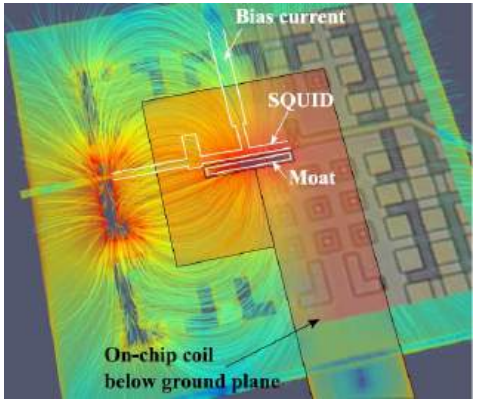


Figure: Configuration of on-chip field coil

[3] K. Jackman and C. J. Fourie. "Flux trapping experiments to verify simulation models". In: *Supercond. Sci. Technol.* 33 (Aug. 2020), p. 105001.

NIST data from Fourie and Jackman (IEEE TAS 2021)

C. J. Fourie and K. Jackman, "Experimental Verification of Moat Design and Flux Trapping Analysis," *IEEE TAS (2021)* doi: 10.1109/TASC.2021.3051582.



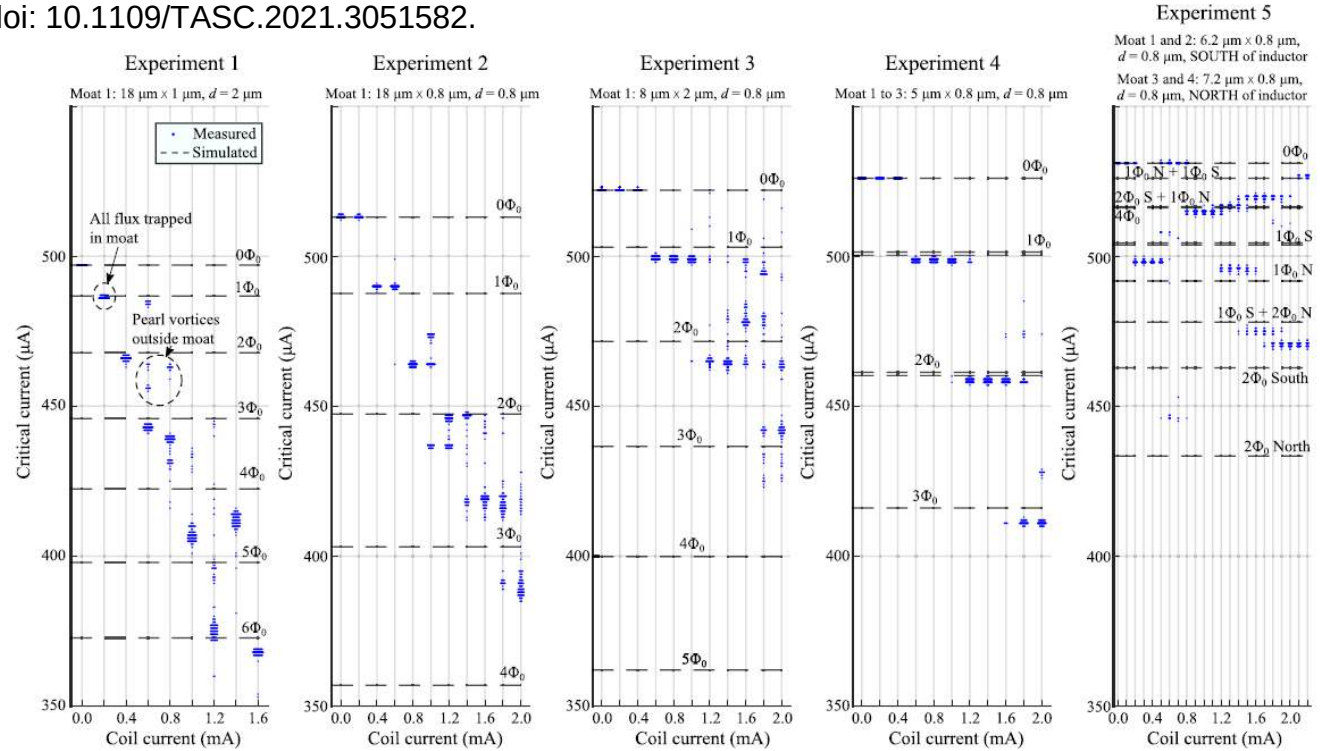


Fig. 9. Critical current of SQUIDs in flux linkage experiments. All simulated trapped flux used flux return path around the edge of the chip.

Data from Manuel Castellanos-Beltran and Adam Sirois, NIST

Slide from Coenrad Fourie, ASC 2020

Compact circuit models for modeling coupling from fluxons in moats to circuit structures have been verified through flux linkage experiments.

With these models, moats can be analysed directly from layouts.

Some conclusions from results:

- Always place more moats than fluxon density per area.
- Double trapping in any moat unlikely for uniform field - Pearl vortices.
- Moats should not run parallel along entire length of an inductor.
- Several staggered moats on opposite sides of inductor (subtract coupling current) better than one long moat.
- Better if moats place perpendicularly to inductors.
- Sky plane with match moats to ground significantly reduces fluxon coupling.

Outline

General guidelines

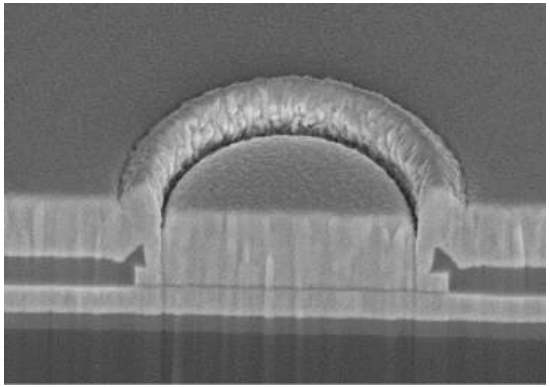
1. Literature
2. Best practices from previous US digital programs
3. Simulation/measurement example from SuperTools

NIST-specific practices

1. Design (no continuous ground planes)
2. Simulation (not presently done)
3. Fabrication
4. Cryostat design and shielding
5. Measurement protocols

SC Group: Fabrication

Bad



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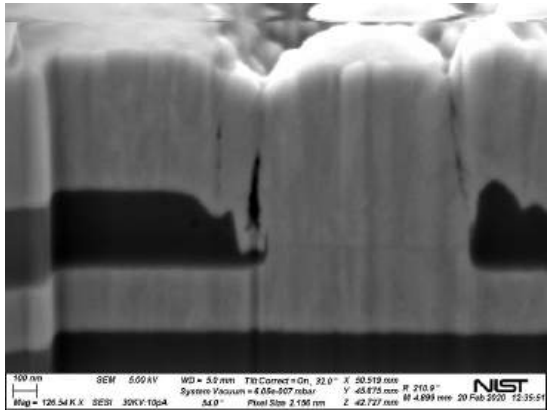
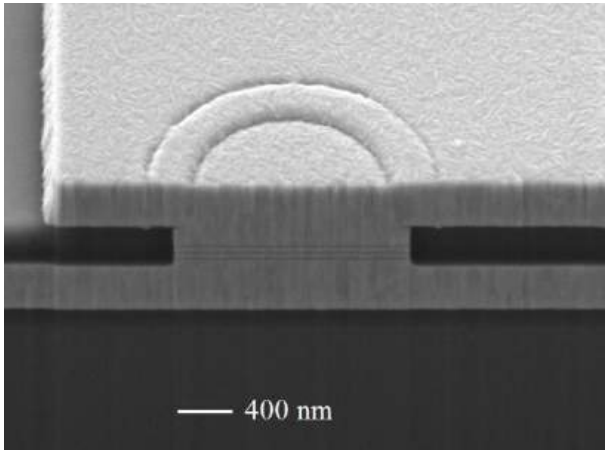
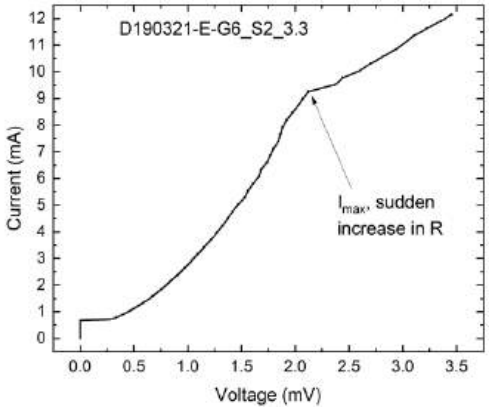
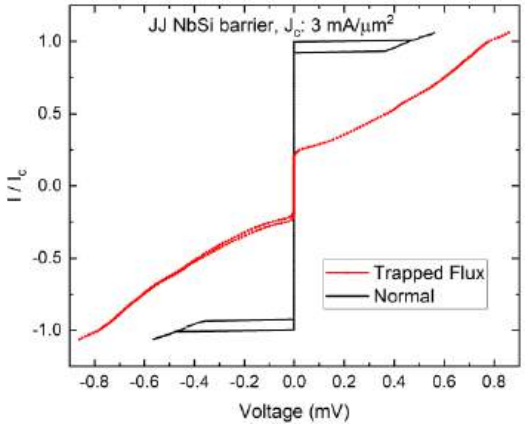


Good







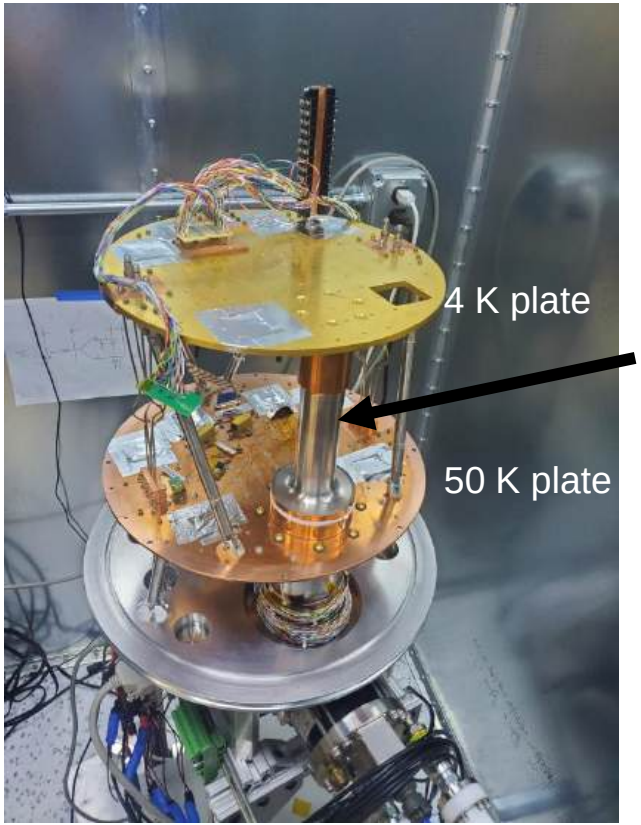
SC Group: Cryostat design and shielding

Immersion Probes

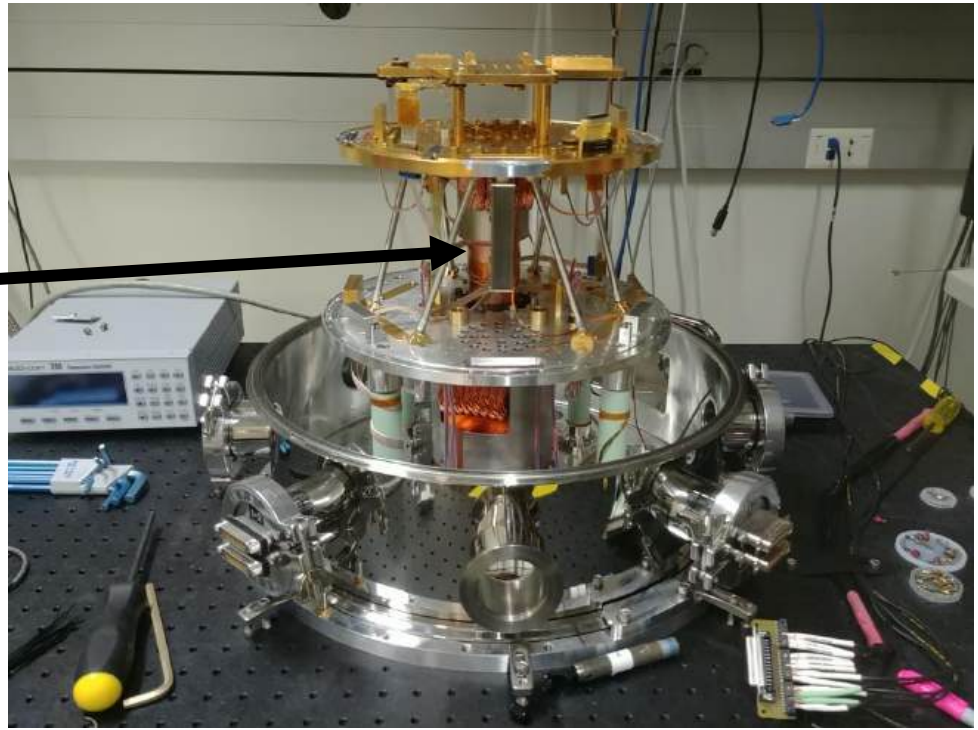
Spring-loaded Cu push block with counter-wound resistive heater

- Ni flash for gold plating of components
- De-Gaussed passive mu-metal shields (Length/dia > 4)
- Non-magnetic stainless LHe dewar – watch weld joints!
- Active field cancellation: Helmholtz coil on dewar

SC Group: Closed-cycle cryostats



2nd Stage Regenerator



B(t) from 2nd Stage Regenerator

GM Cryocooler

S. Fujimoto et al., Cryogenics 35 (1995)

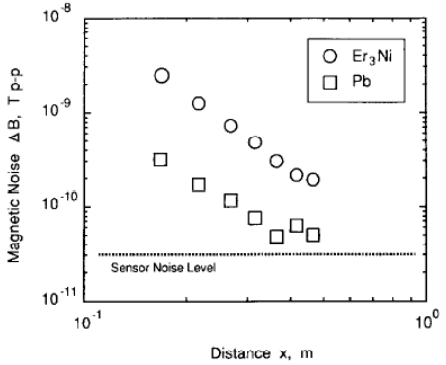


Figure 2 Distance *x versus* magnetic noise ΔB for the flux-gate magnetometer

Pulse Tube

M.J. Eshraghi et al./Cryogenics 49 (2009) 334–339

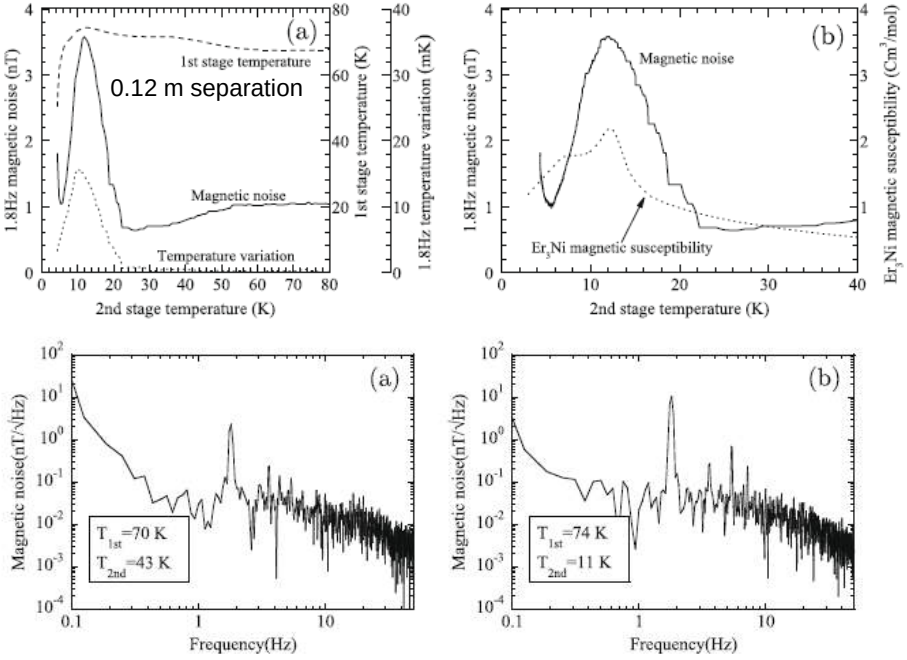


Fig. 3. Magnetic noise spectrum measured by fluxgate magnetometer (a) $T_{2nd} = 43$ K (b) $T_{2nd} = 11$ K.

- Er_3Ni or $HoCu_2$: paramagnetic to antiferromagnetic transition at $T \leq 10$ K.
- Noise source: Temp oscillations + Temperature-dependent magnetic susceptibility

Cryogen-free variable temperature scanning SQUID microscope

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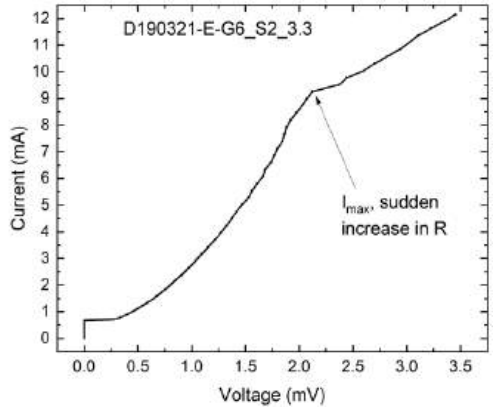
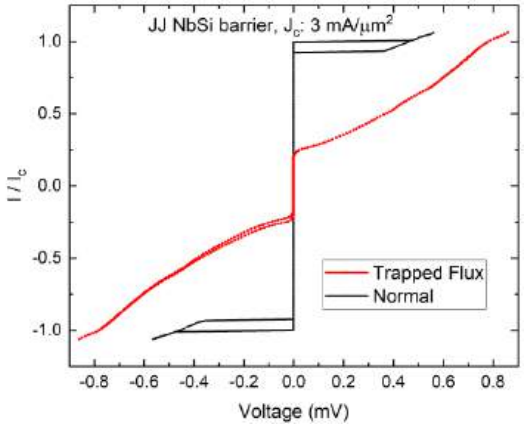
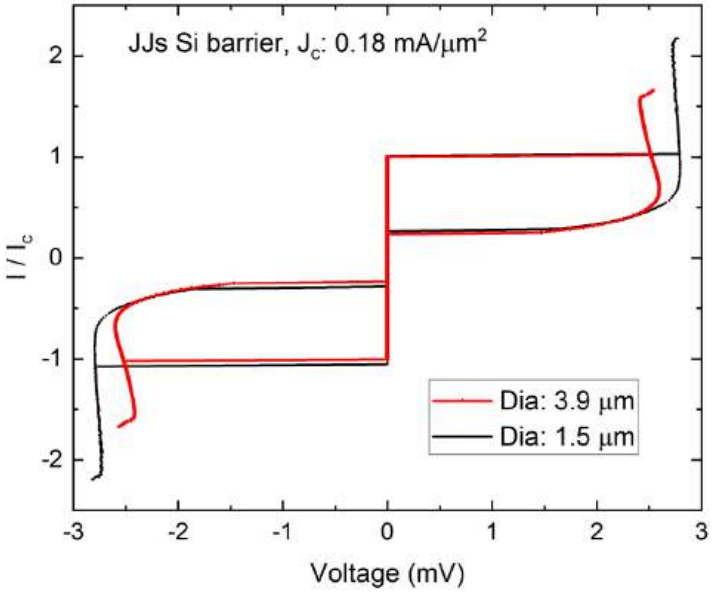
SC Group: Measurement protocols







- Testing at high current leads to heating (previously shown)
- Back-bending at gap voltage
- Indicative of sample heating (high I_c)

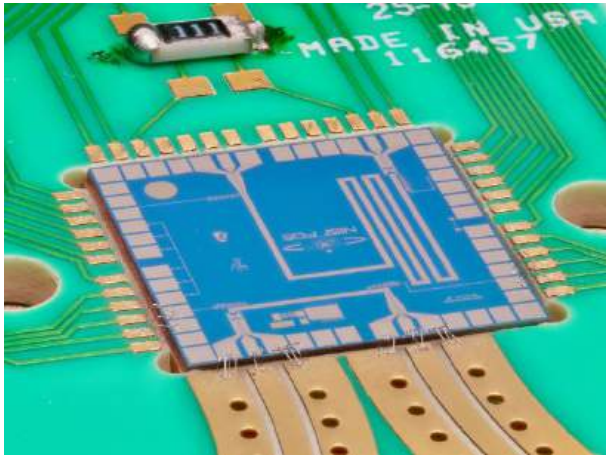
Summary

General guidelines

1. Best practices from previous US digital programs
2. Literature list
3. Simulation/measurement example from SuperTools

NIST-specific practices

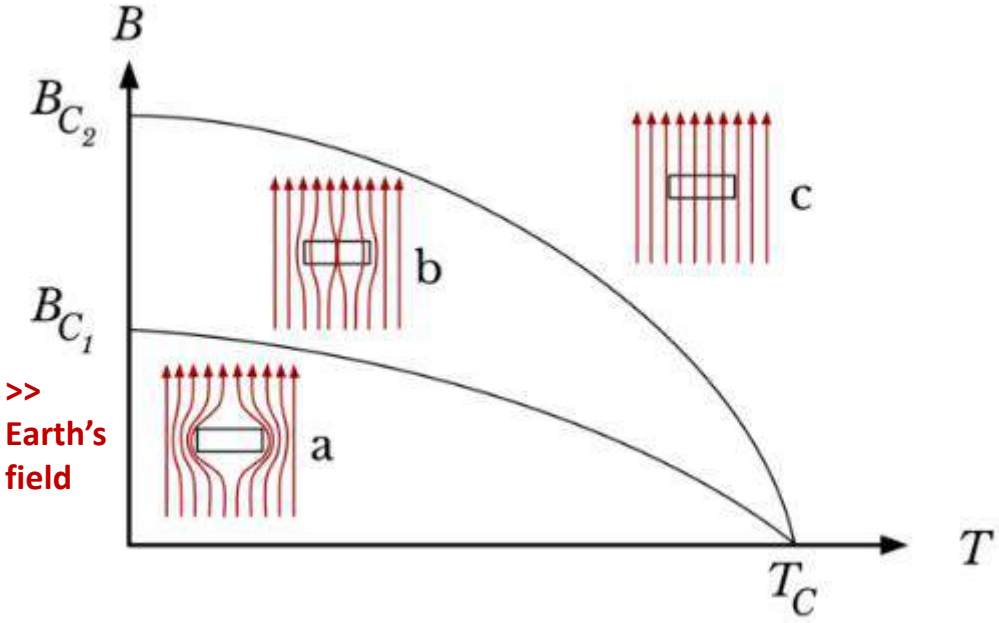
1. Fabrication
2. Cryostat design and shielding
3. Measurement protocols

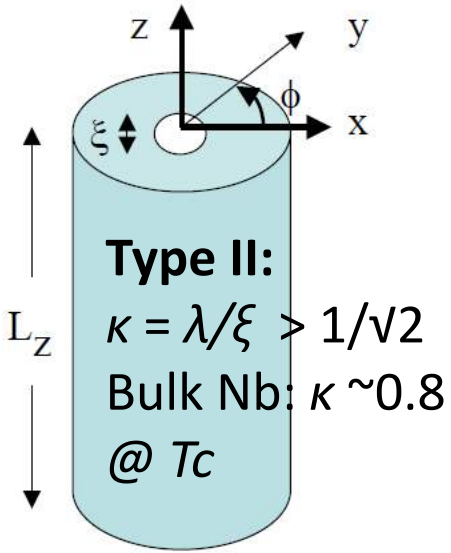


Thank You!

Manuel Castellanos-Beltran, Sam Benz, Paul Dresselhaus, David Olaya, Pete Hopkins

Trapped flux in Bulk Type II superconductors (e.g. Nb)

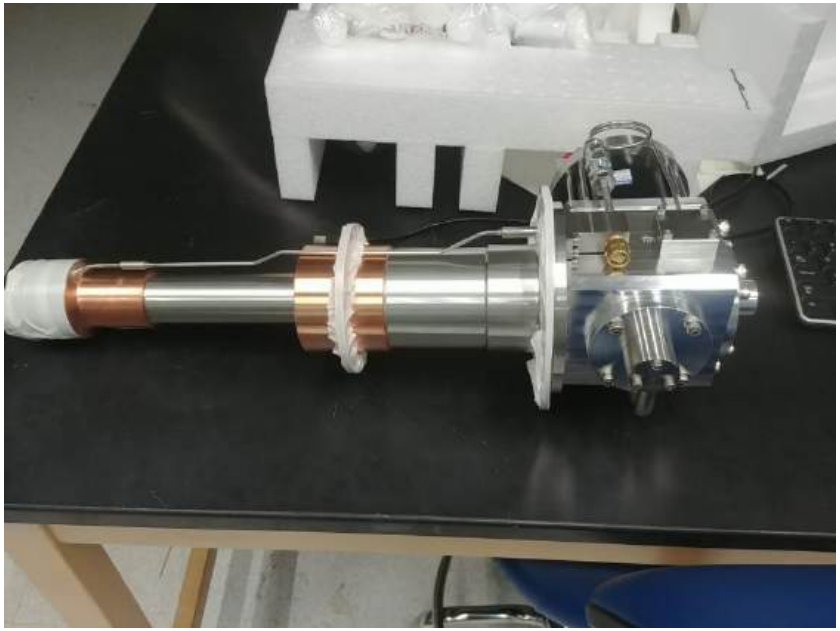




- Abrikosov (1957, Nobel 2003) - Type 2 Superconductors
- *λ= London penetration depth, ξ=coherence length*
- free of imperfections
- Imperfections can pin the flux

Dry cryostats: B Field from GM and Pulse Tubes

GM Cryocooler



Cryogenic Fluxgate Magnetometer