Overview of large-scale AQFP efforts and FSDL plans at Yokohama National University

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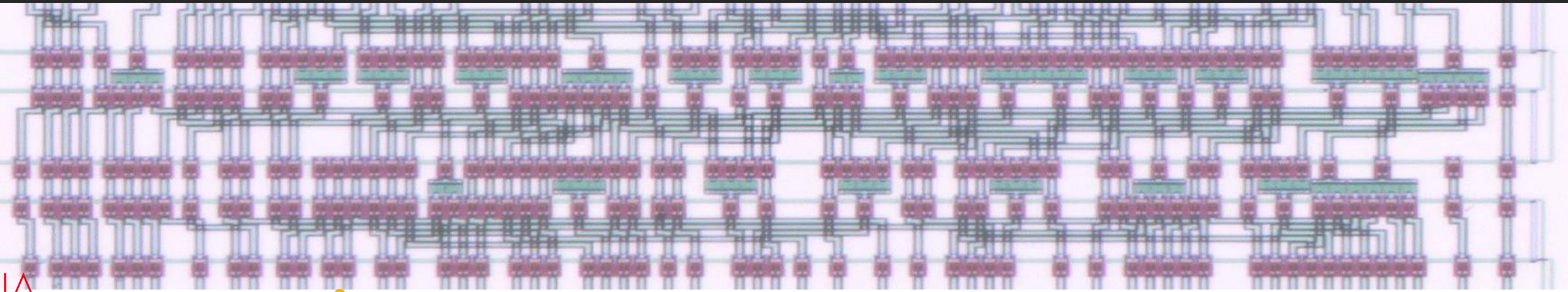


Yoshikawa Group @ YNU

Institute of Advanced Sciences (IAS)
Quantum Information Research Center

Quantum Information Research Center

Institute of Advanced Sciences
Yokohama National University

横浜国立大学
先端科学高等研究院

FSDL Members

Prof. Nobuyuki Yoshikawa

Prof. Yuki Yamanashi

Prof. Christopher Ayala

Prof. Yuki Hironaka

Prof. Zongyuan Li

Haruya Ikeda (student)

Prof. Hongxiang Shen

Prof. Wenhui Luo

Dr. Hideo Suzuki

Dr. Naoki Takeuchi (now @ AIST)

Prof. Olivia Chen (now @ TCU)

Prof. Yuxing He (now @ SWJTU)

Dr. Taiki Yamae (now @ AIST)

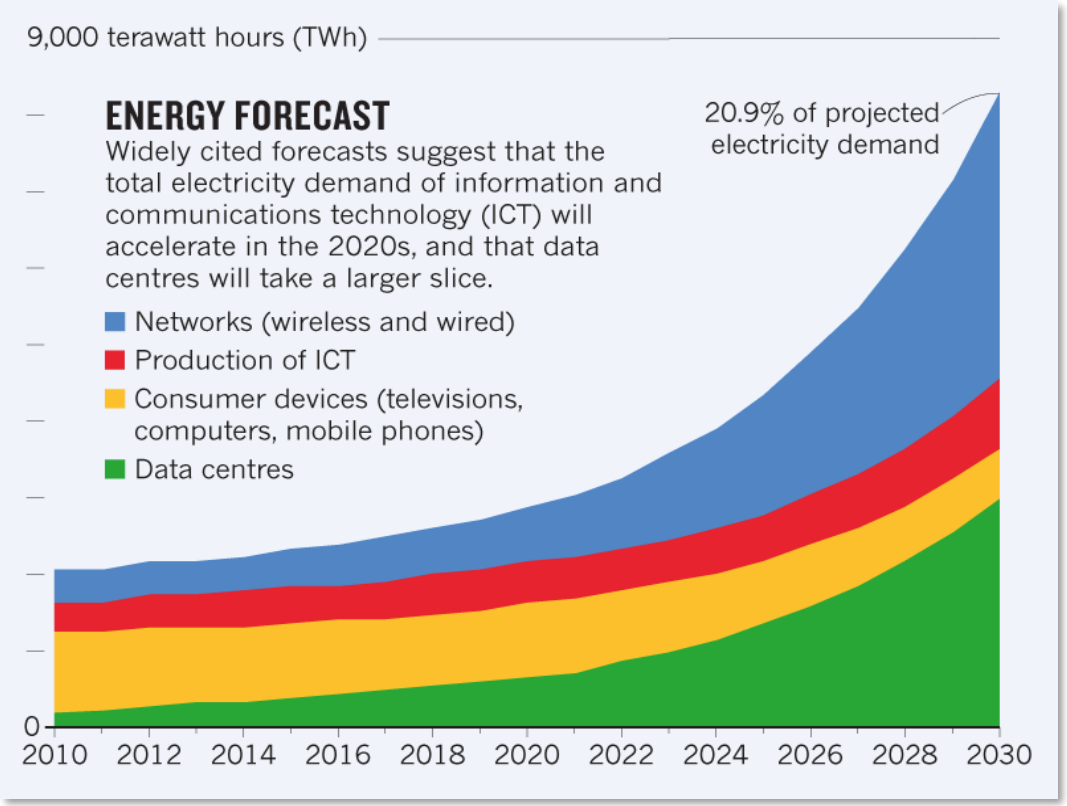
Prof. Lieze Schindler (now @ SU)

Michael Johnston (now @ SARAO)

Motivation

Trend of rising electricity demand of information and communications technology (ICT).

Currently 10% of the total electric power worldwide.



N. Jones, *Nature*, vol. 561, no. 7722, pp. 163–166, Sep. 2018.

Worst-case scenario: ICT could use as much as 50% of global electricity by 2030.

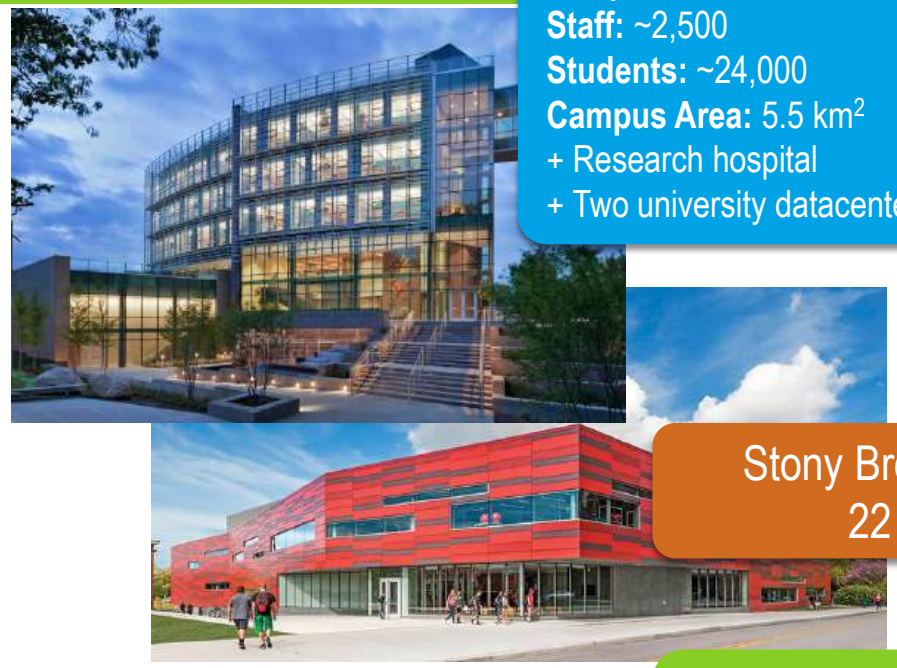
A. S. G. Andrae and T. Edler, *Challenges*, vol. 6, no. 1, pp. 117–157, Jun. 2015.

TechNavio, Data Center Market by Component and Geography - Forecast and Analysis 2022-2026
SKU: IRTNTR40958

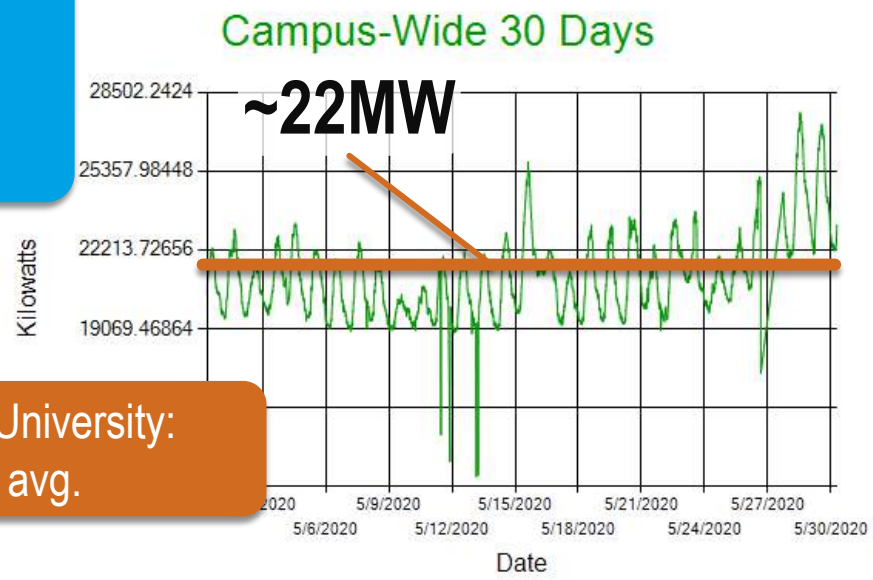
Global market for data centers growing rapidly – **Cybersecurity is a key major challenge.**

Motivation

Stony Brook University
Stony Brook, New York, USA
Staff: ~2,500
Students: ~24,000
Campus Area: 5.5 km^2
+ Research hospital
+ Two university datacenters



https://www.asa.stonybrook.edu/Sustainability/energy/



Stony Brook University:
22 MW avg.

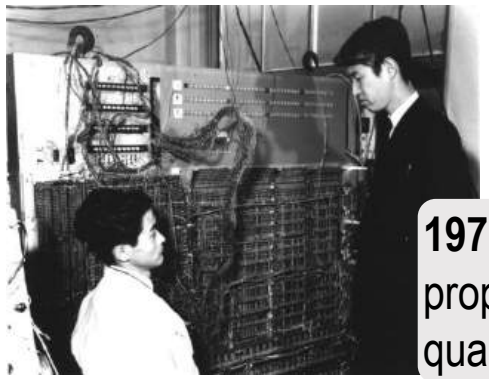
Facebook's datacenter uses
3.8x the power of a university

Facebook Lulea Datacenter:
84 MW avg.

Motivation – Bitcoin (BTC) example

Energy-efficient superconductor electronics (SCE) potentially address power problem in large-scale computing, data centers and cybersecurity.

University of Cambridge Bitcoin Electricity Consumption Index: https://ccaf.io/cbeci/index/comparisons (2023)



Goto (left) and Takahashi with PC-1

1986: DC flux parametron, later renamed to QFP [4]

1976: K. Likharev proposes parametric quantron [3]

Phase mode, RSFQ emerging

2014: IARPA C3; **2017:** IARPA SuperTools

SCE μPro: SPELL, FLUX-1, CORE, LSRDP, FRONTIER

Energy-efficient SCE logic

1950 1960 1970 1980 1990 2000 2010 2020 2030s…

MOS IC ramps up

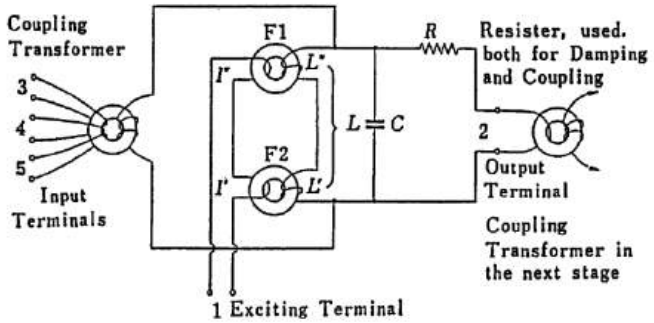
CMOS takes over NMOS

FSDL as enabler

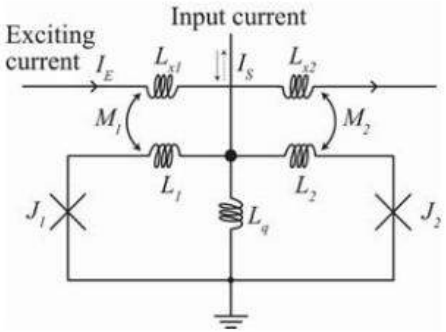
1954: Eiichi Goto invents parametron [1]
1958: Parametron-based PC-1 computer
1960: Parametron-based Esaki Diode pair logic (precursor to the QFP) [2]

2011: N. Yoshikawa (YNU) first proposed the adiabatic QFP (AQFP) [5]

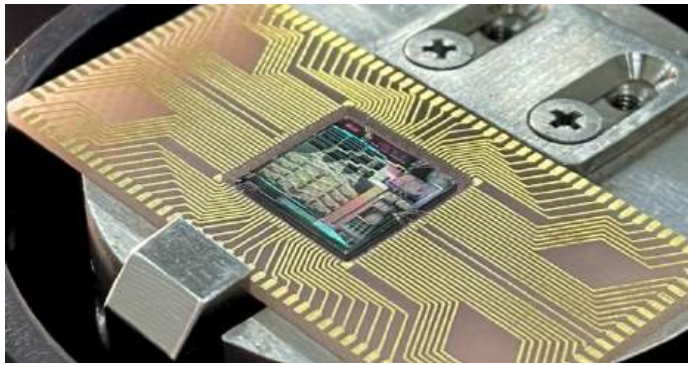
2020: First adiabatic superconductor μprocessor MANA using AQFPs [6]



Parametron schematic



Adiabatic quantum-flux-parametron

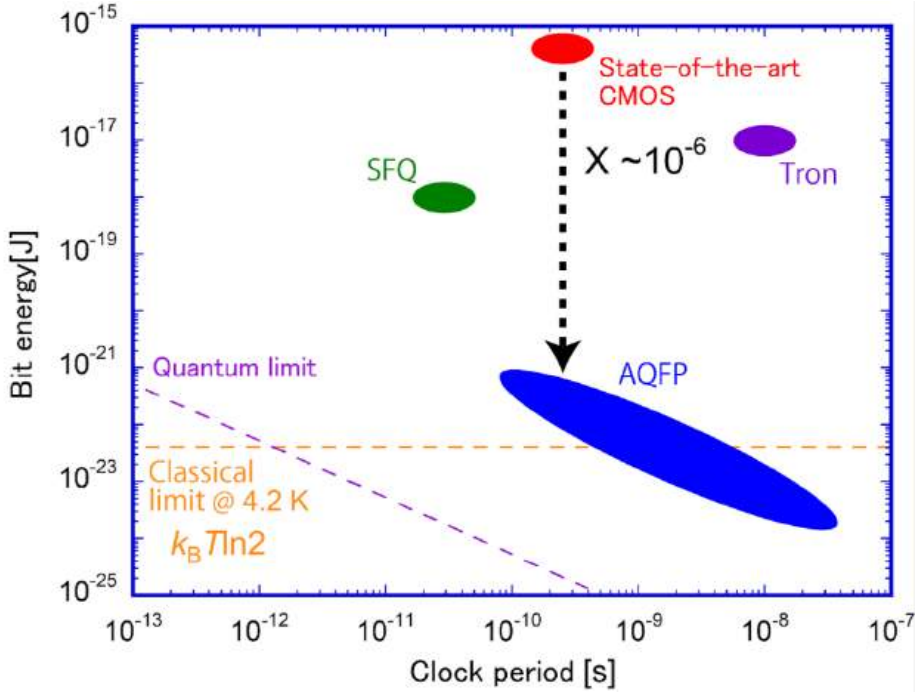


MANA AQFP microprocessor

[1] E. Goto, *Proceedings of the IRE*, vol. 47, no. 8, pp. 1304–1316, Aug. 1959.
[2] E. Goto *et al.*, *IRE Trans. on Elec. Comp.* vol. EC-9, no. 1, pp. 25–29, Mar. 1960.
[3] K. Likharev, *IEEE Trans. Magn.*, vol. 13, no. 1, pp. 242–244, Jan. 1977.
[4] E. Goto and K. F. Loe, *Dc Flux Parametron*. World Scientific, 1986.
[5] N. Yoshikawa *et al.*, 2011 SSDM, doi: 10.7567/ssdm.2011.j-8-3.
[6] C. L. Ayala *et al.*, *IEEE J. Solid-State Circuits*, vol. 56, no. 4, pp. 1152–1165, Apr. 2021.

AQFP logic for computing

- **A**diabatic **q**uantum-**f**lux-**p**arametron (AQFP) logic
  - Composed of a pair of Josephson junction (JJ) superconductor devices
  - Extremely small bit energy << $I_c\Phi_0$
    - Very small switching energy due to adiabatic operation
    - 1.4 zJ per JJ at 4.2 K in experiment [1]
  - High gain
    - 10-50x gain from μA's of input current
  - High robustness
  - Clock speeds on par with state-of-the-art CMOS logic (5-10GHz)



After cooling overhead [2], **~80x more efficient** than 7nm FinFET with V_{DD} = 0.8V [3]

[1] N. Takeuchi et al., Appl. Phys. Lett., vol. 114, no. 4, p. 042602 (2019)
[2] D.S. Holmes et al., IEEE TAS, 23, no.3, (2013)
[3] A. Stillmaker et al., Integration. 58, pp. 74-81 (2017)

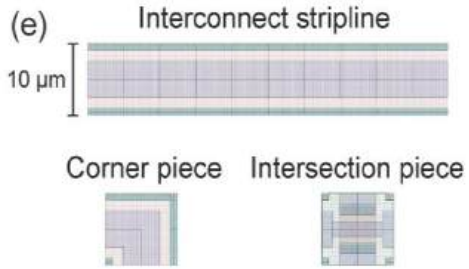
AQFP logic a promising candidate for energy-efficient computing.

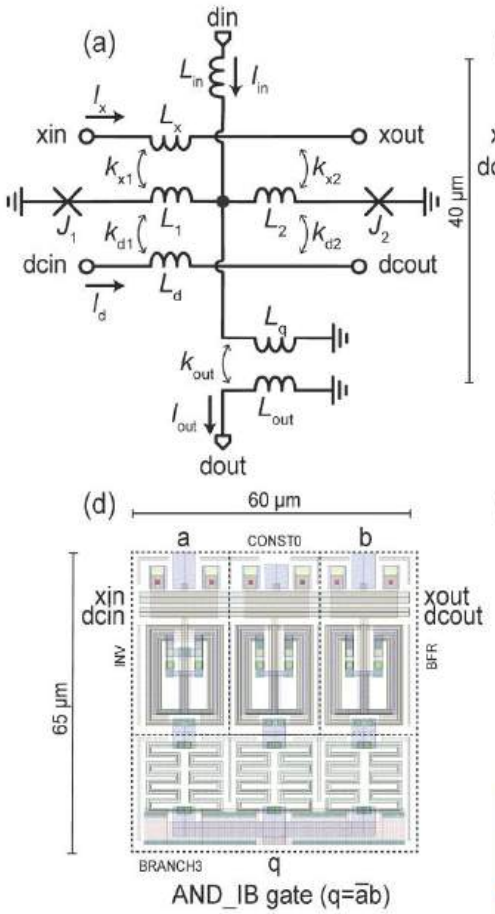
Cell library: minimalist design

L_{in} = 1.13 pH
L_x = 5.67 pH
L_d = 6.16 pH
L_1, L_2 = 1.53 pH
L_q = 7.88 pH
L_{out} = 31.9 pH
k_{d1},k_{d2} = -0.154
k_{x1},k_{x2} = -0.209
kout = -0.515
J_1, J_2 = 50 μA

Excitation/clock lines are 50Ω microstriplines

Interconnect are shielded striplines

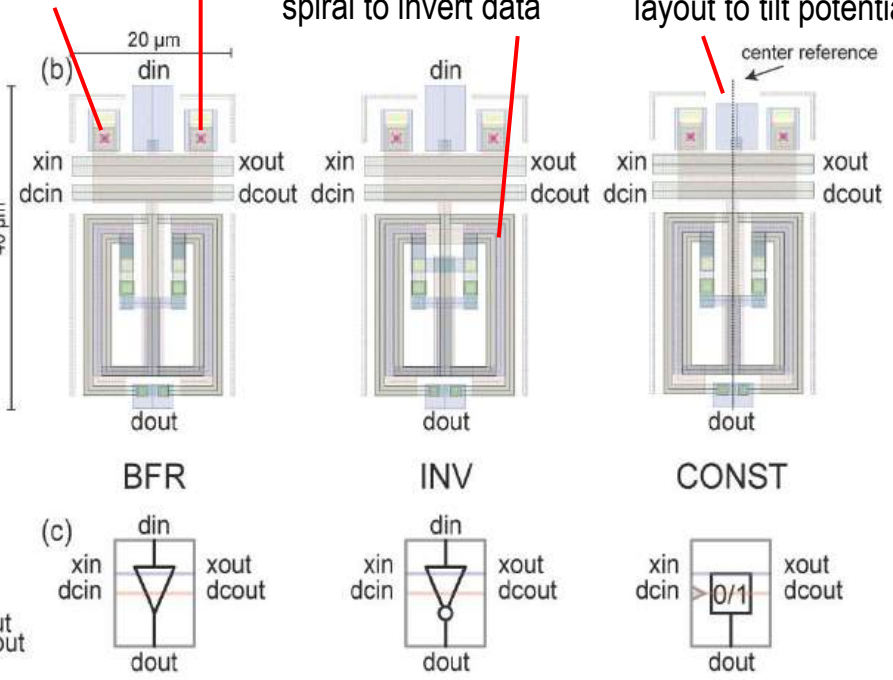


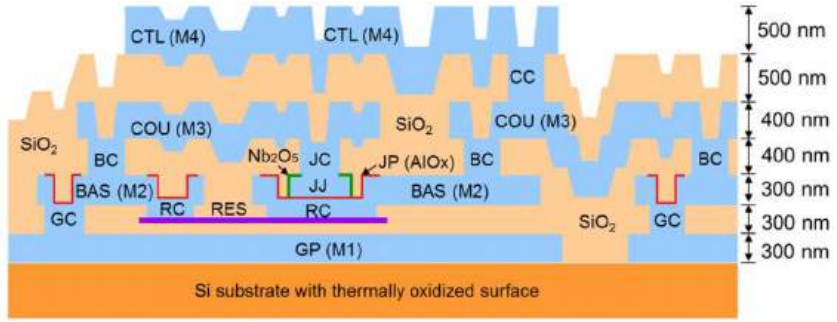


Josephson junctions (JJs)

Reverse transformer spiral to invert data

No input + asymmetric layout to tilt potential





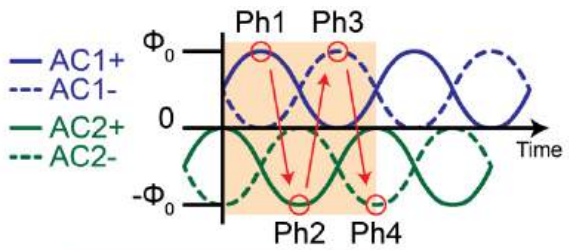
4-layer Nb/AlO_x/Nb 10 kA/cm^2 high-speed standard process (HSTP) by AIST, Tsukuba, Japan

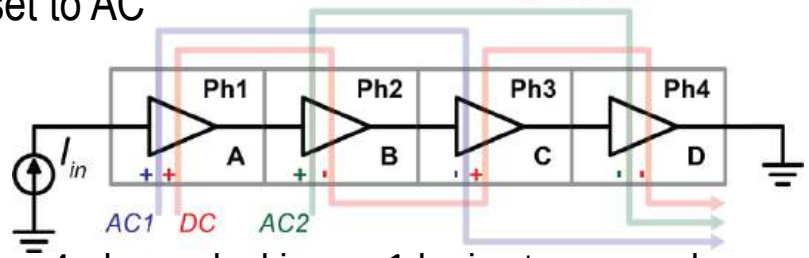
N. Takeuchi *et al., Supercond. Sci. Technol.*, vol. 30, no. 3, p. 035002, Mar. 2017.
C. L. Ayala *et al.*, *Supercond. Sci. Technol.*, vol. 33, no. 5, p. 054006, Mar. 2020.

Data propagation in AQFP logic

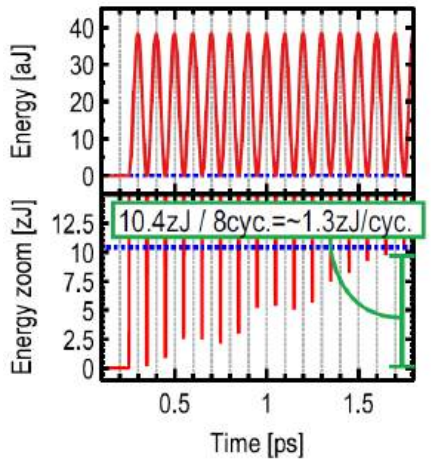
90° phase shift btw **AC1** & **AC2**

DC provides +/- offset to AC

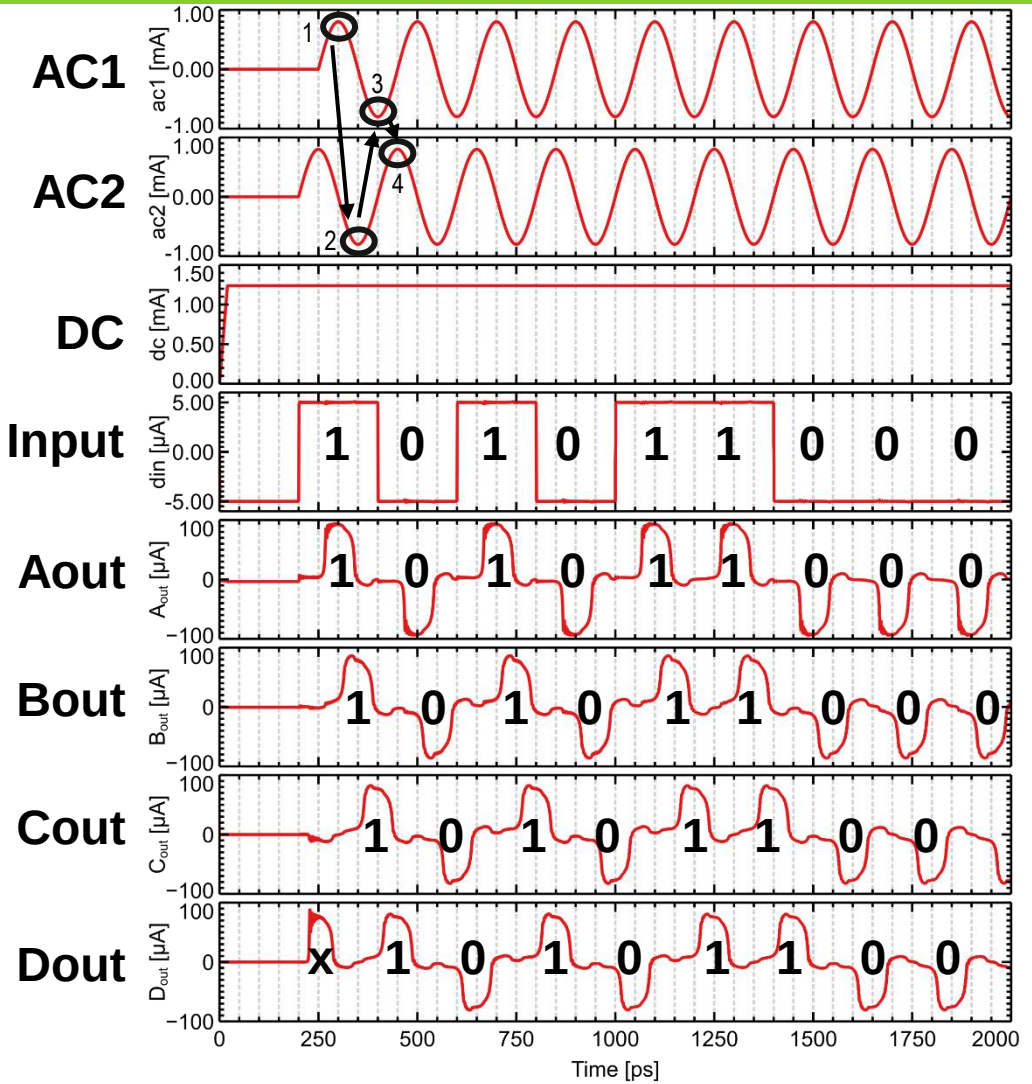




4-phase clocking → 1 logic stage per phase



Adiabatic switching in JSIM. Measured to be 1.4zJ/cyc. at 5 GHz [1].

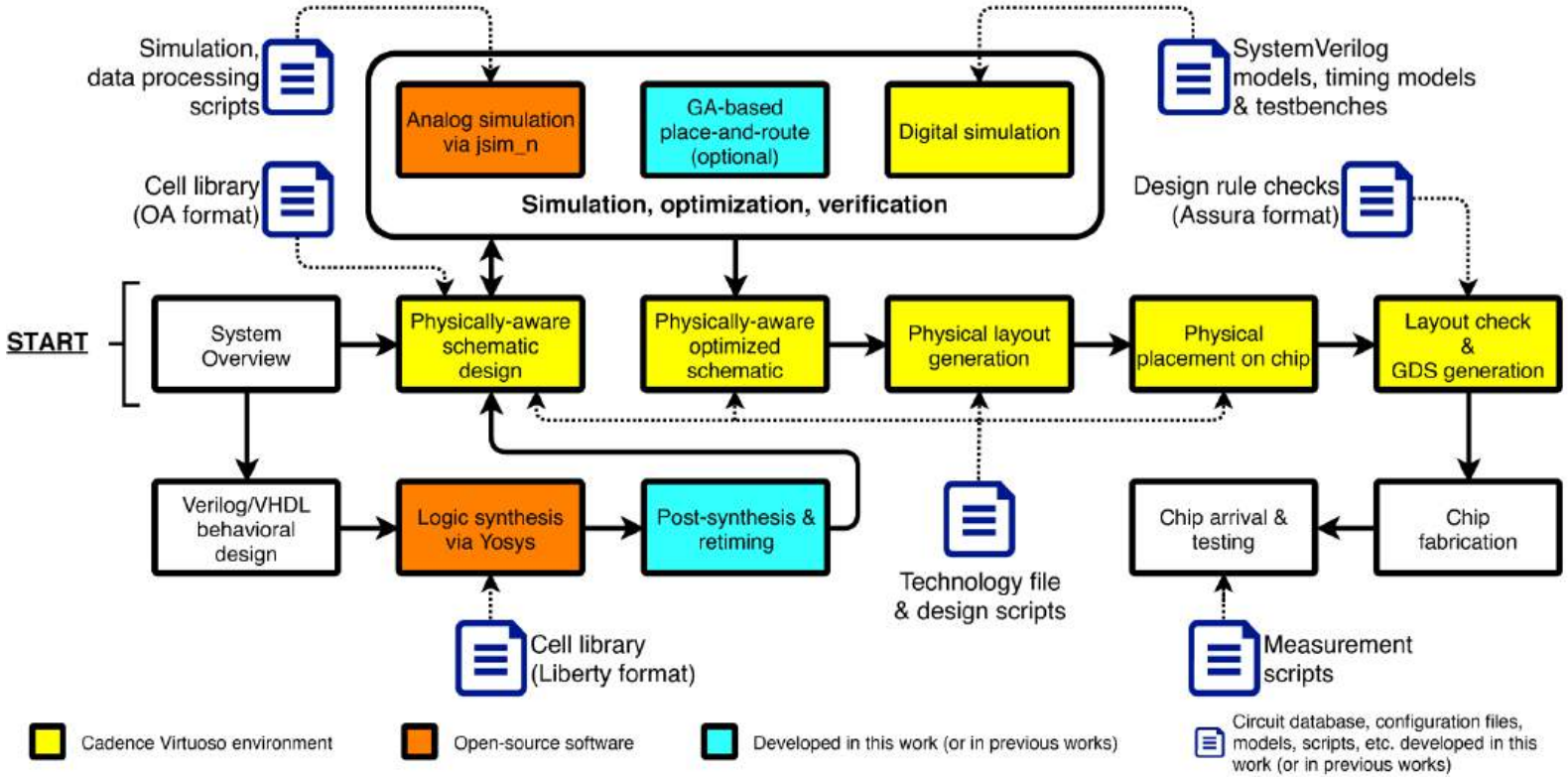


Simulation of four buffers in series in JSIM.

http://www0.sun.ac.za/ix/?q=tools_jsim

[1] N. Takeuchi et al., *Appl. Phys. Lett.*, vol. 114, no. 4, p. 042602, Jan. 2019.

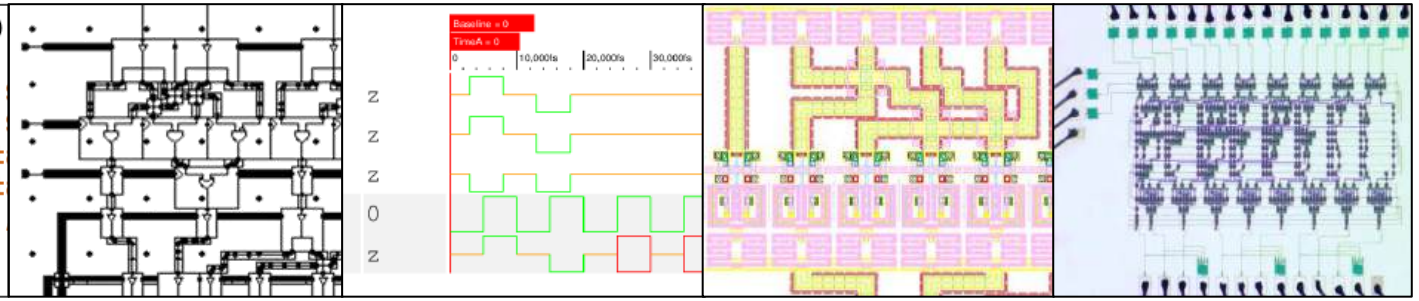
Semi-custom AQFP design flow



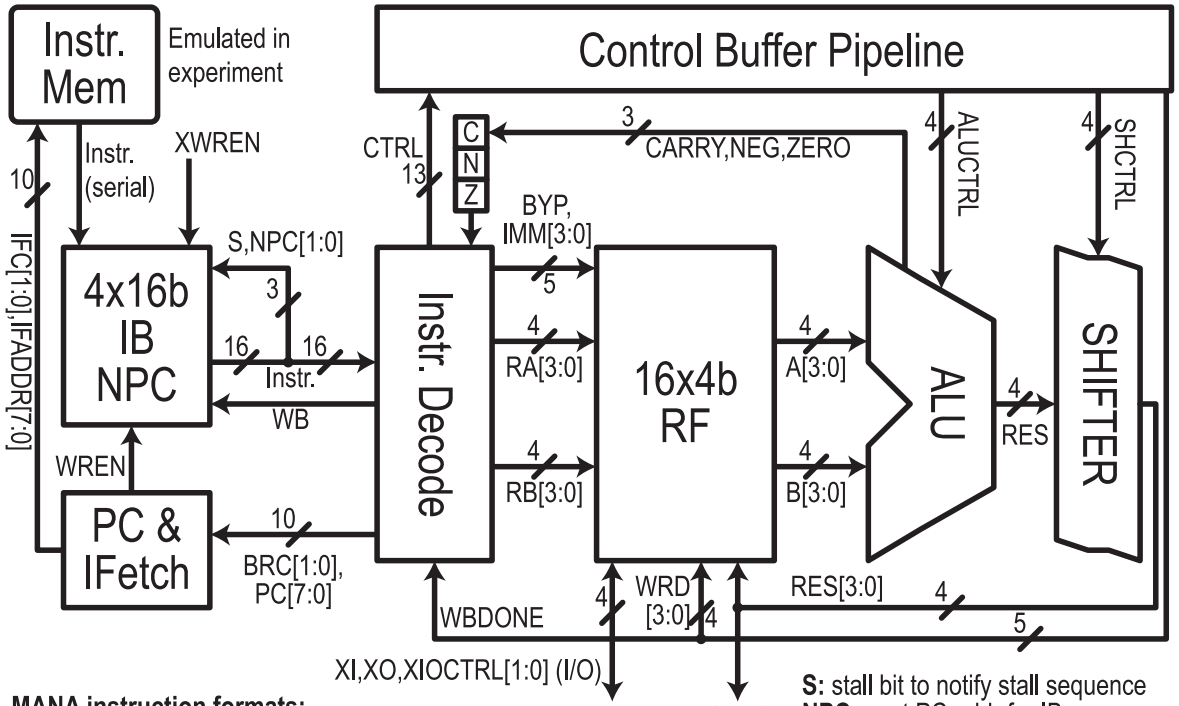
C. L. Ayala *et al.*, *Supercond. Sci. Technol.*, vol. 33, no. 5, p. 054006, Mar. 2020.

Verilog/VHDL | Schematic | Digital Sim. | Layout | Chip

```
always @(data_in, sh_ctrl, sh_amt)
  case(sh_ctrl)
    2'b00 : data_out = data_in <<
    2'b01 : data_out = data_in >>
    2'b10 : data_out = $signed(dat
    2'b11 : data_out = $signed(dat
    default : data_out = data_in;
  endcase
end
```



Towards AQFP microprocessors: MANA



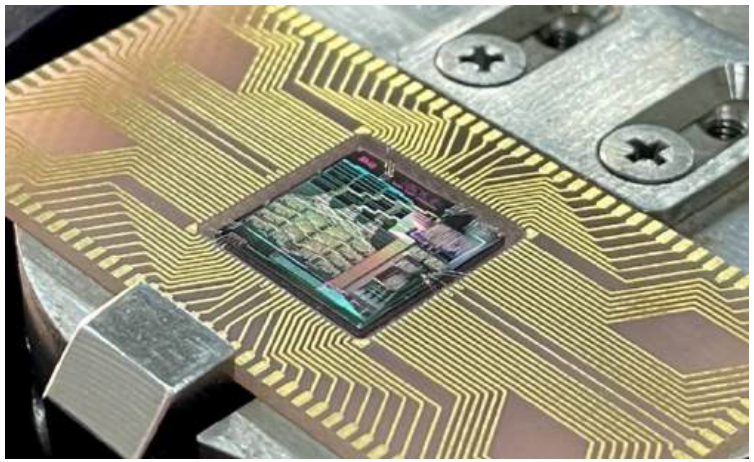
MANA instruction formats:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
S	NPC		OPCODE					IMM				RB				Immediate format
S	NPC		OPCODE					BRC/JMP ADDR								Branch/jump format
S	NPC		OPCODE					RA				RB				ALU format
S	NPC		OPCODE					SOP		AMT		RB				Shifter format
S	NPC		OPCODE					MEM								Memory access format

S: stall bit to notify stall sequence
NPC: next PC addr for IB
OPCODE: opcode of instr.
IMM: immediate value
BRC/JMP: branch/jump addr.
RA: reg. A addr.
RB: reg. B addr. (also destination)
SOP,AMT: shift opcode and amount
MEM: Mem. addr. for data.

MANA – Monolithic Adiabatic iNtegration Architecture

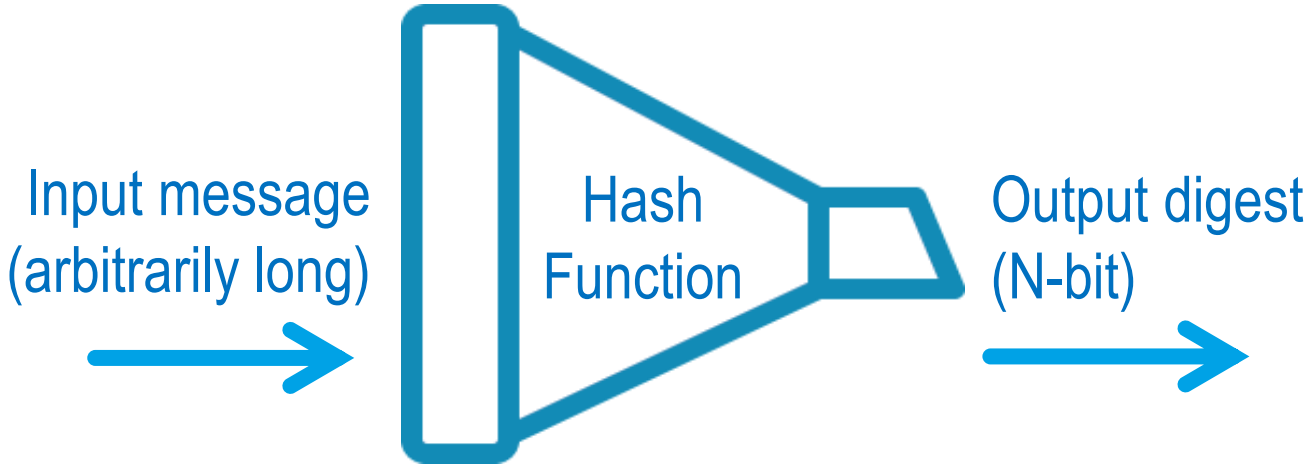
- **Goal:** Demonstrate AQFP can do both logic and memory
- RISC-like datapath + dataflow-like control
- 21,460 JJs in 1 x 1 cm^2 chip; 30 fJ/op at RT @ 5 GHz



Cryptography: hashing

In what application can we leverage SCE technology today?

- How about cryptography – hashing?
  - $h : \{0, 1\}^* \longrightarrow \{0, 1\}^n$
  - Input: "message" arbitrarily long binary input
  - Output: "digest" fixed length (*n*) binary output
    - Ideally a unique signature for the input message
  - Similar inputs ⇒ dissimilar outputs
  - Ideally difficult to reverse engineer input using output



Uses:

- O(1) data structure in programs (Hash Table)
- Digital signatures
- Encryption/cybersecurity
- Cryptocurrency

Architecture implementation properties:

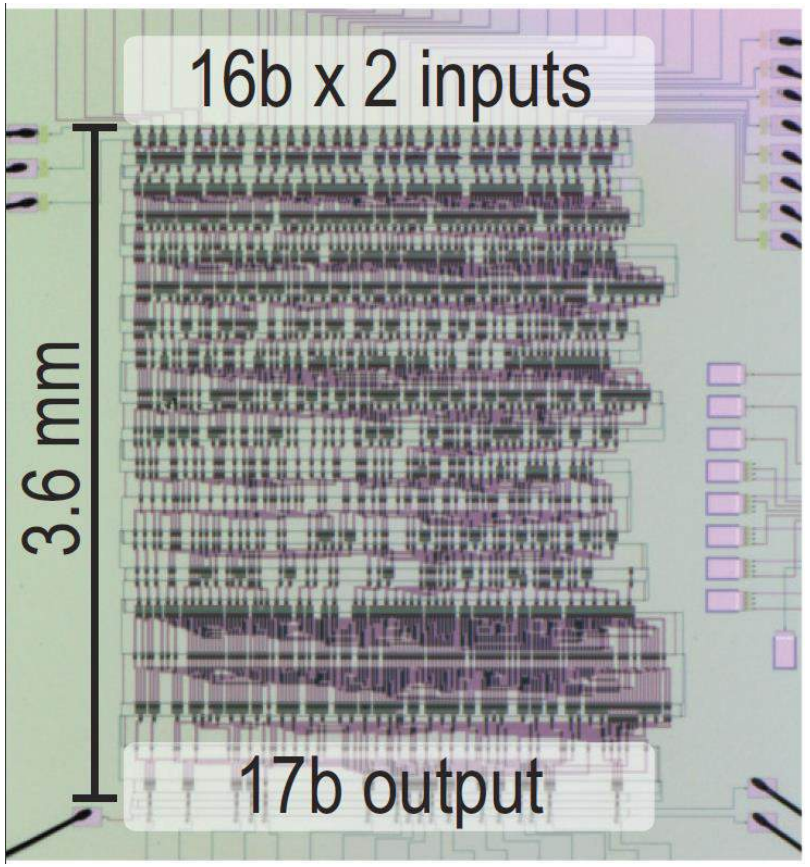
- Data feedback is typically well-controlled
- Control is simple, usally defined as fixed rounds/iterations (counters)
- Usually, no need for centralized memory during hashing

Secure Hashing Algorithms (SHA)

Algorithm	Year	Output Size	State Size	Operations	Collisions Found?
SHA-0	1993	160-bit	160-bit	AND, XOR, OR, ROT, ADD32	Yes ($\leq 2^{34}$ evaluations)
SHA-1	1995	160-bit	160-bit	AND, XOR, OR, ROT, ADD32	Yes ($< 2^{63}$ evaluations)
SHA-2 (Bitcoin mining)	2001	256-bit	512-bit	AND, XOR, OR, ROT, SHR, ADD32	No (2^{128} evaluations)
SHA-3 (SHA3-256)	2015	256-bit	1600-bit*	AND, XOR, ROT, NOT	No (2^{128} evaluations)

SHA3/Keccak (“Ket-chak”) algorithm won the NIST hash function competition in 2012

SHA-3 is paramterizable*, simple, and modern – good candidate for implementation.

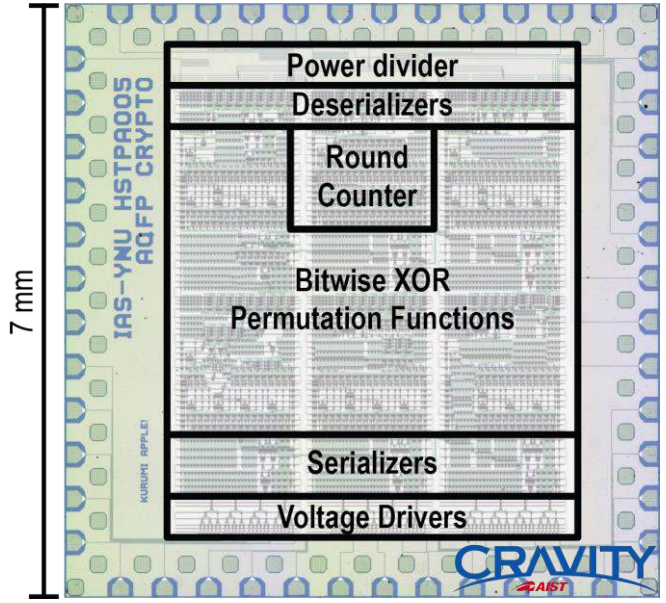


16-bit AQFP Kogge-Stone adder component [1]

[1] T. Tanaka et al, “A 16-bit parallel prefix carry look-ahead Kogge-Stone adder implemented in adiabatic quantum-flux-parametron logic,” IEICE Transactions on Electronics, vol. E105–C, no. 6, Jun. 2022.

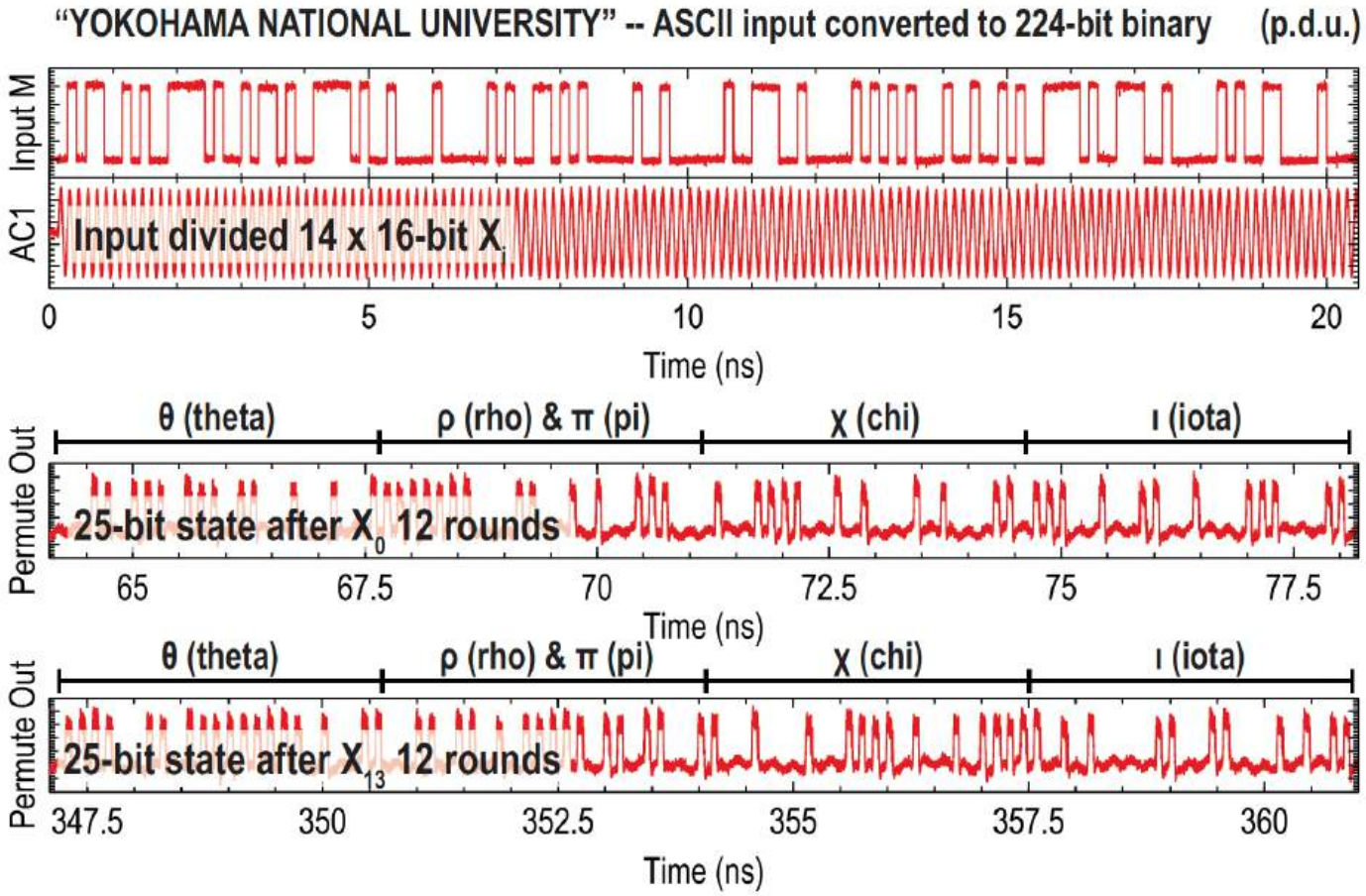
Measurement of SHA-3 permutation block

C. L. Ayala et al., "Multi-GHz zeptojoule computing using emerging adiabatic superconductor circuits," DOI: 10.1109/isvlsi61997.2024.00106



Chip No.	AC Margin (%)	Max. Freq. (GHz)	Permute BER	Shift Register BER
1	+16 / -12	7	10^{-4}	10^{-18}
2	+12 / -12	4.5	10^{-3}	10^{-17}
3	+14 / -12	5	10^{-4}	10^{-18}
4	+12 / -10	4	10^{-2}	10^{-17}

(l=0 b=25 r=16 c=9 n=12)



JJ count: 13,008 JJs (state size=25 bits)
Chip: 7 mm x 7 mm, 48 pad
Active circuit area: 5.0 mm x 5.6 mm
Maximum operation: 7 GHz
AC margins: +16% / -12%

- Complex test – PyVISA used to help automate experiment
- First +10k JJ AQFP chip at GHz speeds – 4 / 6 chips
- BER rather high on the permutation outputs (10^{-4}) at 7 GHz
- BER on debug shift-registers (SR) reasonable (10^{-18}) at 7 GHz

Limitations of SHA-3 demo

- State size *b* is only 25-bits
- Increasing state size and performance requires…

Area efficiency

- Advanced process such as MIT LL SFQ5ee [1]
- Directly coupled QFP (DQFP) + π-JJs [2]
- Novel compact memory
- MAJ5+ logic gates

Latency / clock distribution

- Low latency clocking [3,4]
- Power-clock H-tree distribution

Interconnect drivability

- Boosters for long interconnect
- Impedance matched lines

Flux trapping

- Detailed analysis and better systematic moat designs [5, 6]

[1] Y. He *et al.*, *Supercond. Sci. Technol.*, vol. 33, no. 3, p. 035010, Feb. 2020.
[2] N. Takeuchi *et al.*, *Supercond. Sci. Technol.*, vol. 33, no. 6, p. 065002, May 2020.
[3] N. Takeuchi *et al.*, *Appl. Phys. Lett.*, vol. 115, no. 7, p. 072601, Aug. 2019.
[4] Y. He *et al.*, *Appl. Phys. Lett.*, vol. 116, no. 18, p. 182602, May 2020.
[5] C. J. Fourie *et al.*, *IEEE Trans. on Appl. Supercond.*, vol. 30, no. 6, pp. 1–9, Sep. 2020.
[6] L. Schindler *et al.*, *IEEE Trans. on Appl. Supercond.*, 2024, accepted.
[7] IARPA SuperTools research program

Foundations of Superconducting Logic (FSDL)

DEVCOM Army Research Laboratory, in collaboration with the Laboratory for Physical Sciences (LPS), is soliciting proposals for foundational research in superconducting electronics (SCE). SCE is a promising technology for high-speed and energy-efficient digital circuits, but scaling towards denser and more reliable systems has been slow. The goal of the Foundations of Superconducting Digital Logic (FSDL) program is to uncover foundational issues limiting the progress of this technology and to pursue innovative research into overcoming these issues across topics such as materials, Josephson junctions, flux trapping, and architecture. FSDL aims to provide the foundation to enable breakthroughs in circuit density and reliability for future SCE-based systems.

- URL: https://arl.devcom.army.mil/collaborate-with-us/opportunity/foundations-of-superconducting-digital-logic-fsdl/
- Kicked off: May 2024
- 4-year program with several performer teams
- YNU is on a performer team led by UC Riverside (Prof. Shane Cybart) along with partners at University of Maryland (Prof. Steven Anlage) and Stanford University (Prof. Kent Irwin, Prof. Kathryn Moler)

YNU's FSDL Plans

Flux trapping investigation

- Design and fabrication of SQUID, AQFP/RSFQ and PTL test structures featuring various moat configurations to investigate the vortex trapping effects.
- Distribute design samples to RF near-field nonlinear microwave microscope (NLMM, UMD) and Scanning SQUID Microscopy (Stanford) groups.
- Measure flux trapping effects in design samples and correlate with microscopy data.

Circuit editing

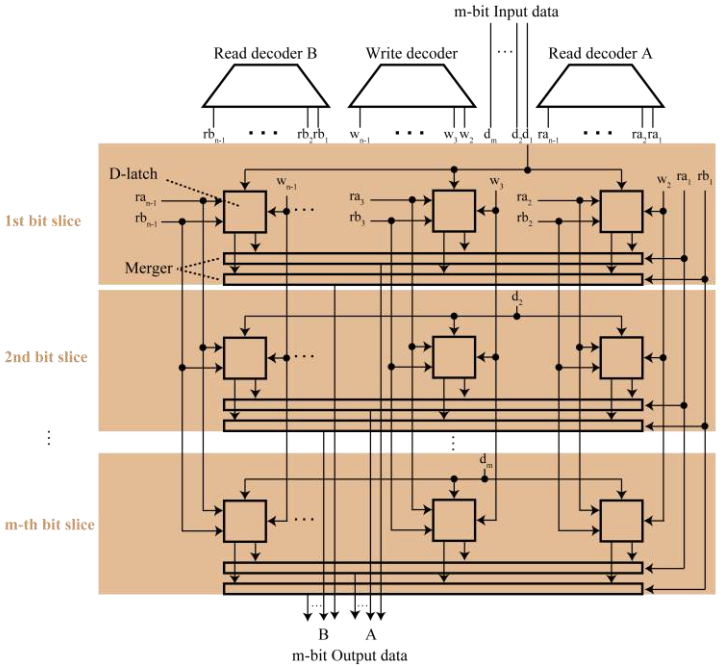
- Design and fabrication of aforementioned circuits suitable for focused ion beam (FIB) circuit editing.
- Distribute design design samples to FIB group (UCR).
  - Modify critical currents, improve symmetry, repair lines, add new nano-moats/pinning sites
- Measure changes (improved margins, reduced offsets, etc.) due to FIB.

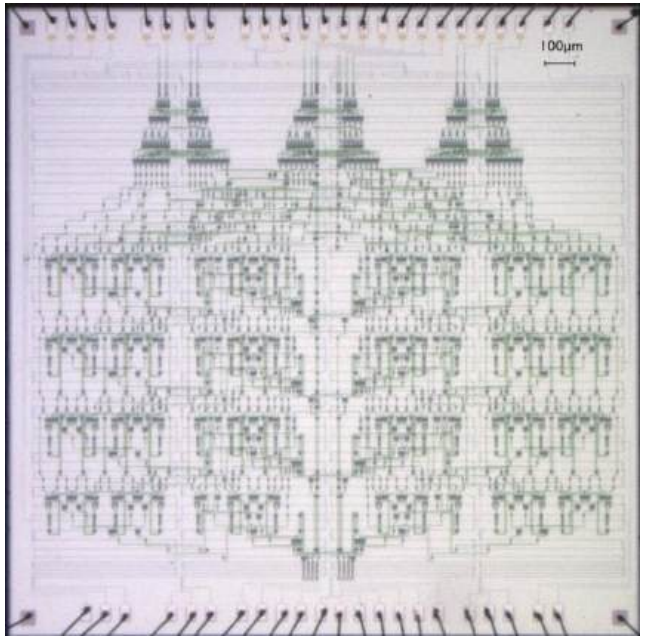
Putting it all together

- Leverage microscopy data, electrical measurement data, and FIB-based circuit improvements to establish new design guidelines to be implemented in next generation standard cells.

Flux trapping in an AQFP register file

Block diagram and chip photo: a 16-word by 4-bit AQFP register file





- With three input and two output ports
- Circuit size: 6.8 mm x 6.8 mm
- Total junction number: 6,438 JJs

Examples of low-speed test results

Test results after the initial cool-down

HSTPA004 No.2 G4		Address number																Corrects /Addresses
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Data output A	D_{a1}	C	C	C	C	C	C	W	W	C	C	C	C	C	C	C	W	13/16
	D_{a2}	C	C	C	C	C	C	C	W	C	C	C	C	C	C	C	C	15/16
	D_{a3}	C	C	C	C	W	C	C	W	C	C	W	C	C	W	C	U	11/16
	D_{a4}	U	C	U	U	U	U	U	W	U	U	U	C	U	C	U	W	3/16
Data output B	D_{b1}	C	C	C	C	C	C	C	C	C	W	C	C	C	C	C	W	14/16
	D_{b2}	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	W	15/16
	D_{b3}	C	C	C	C	W	C	W	U	C	W	W	U	C	W	C	U	8/16
	D_{b4}	C	C	U	U	W	U	W	U	W	W	W	C	U	C	C	W	5/16

Test result after the second cool-down

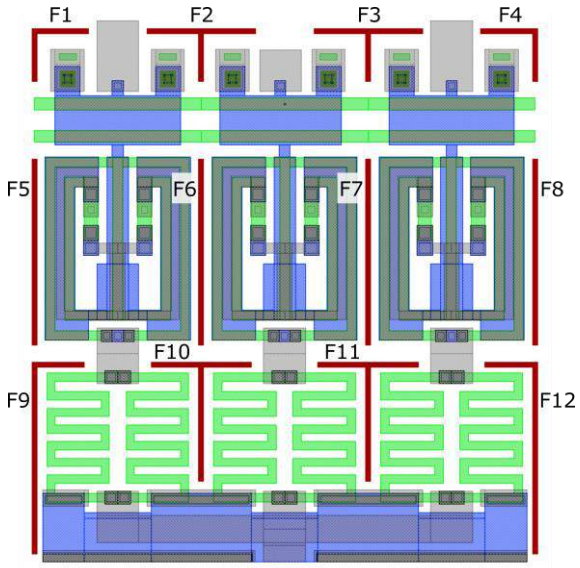
HSTPA004 No.2 G4		Address number																Corrects /Addresses
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
Data output A	D_{a1}	W	C	0	C	C	C	0	C	C	C	C	C	W	W	C	C	11/16
	D_{a2}	W	C	0	C	C	C	C	C	C	C	C	C	W	W	C	C	12/16
	D_{a3}	W	C	0	C	C	C	0	C	C	C	W	0	W	W	C	C	9/16
	D_{a4}	W	C	0	C	C	C	C	C	C	C	0	0	W	W	C	0	9/16
Data output B	D_{b1}	W	C	C	C	C	C	U	U	W	W	W	U	W	W	U	U	5/16
	D_{b2}	W	C	C	C	C	C	C	C	W	W	W	W	W	W	W	W	7/16
	D_{b3}	C	C	0	C	0	C	0	C	C	W	W	W	C	W	C	W	8/16
	D_{b4}	W	C	C	C	C	C	C	C	W	W	W	W	W	W	W	W	7/16

C: correct operation, W: wrong operation, U: unstable operation

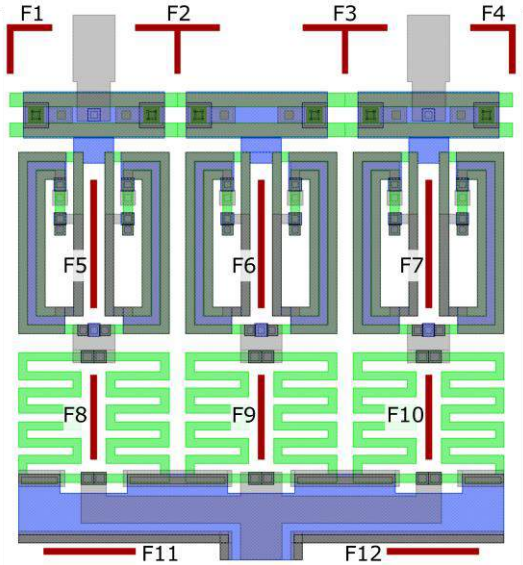
Flux trapping substantially affects the circuit operation.

Moat analysis of AQFP OR cell using InductEx

Standard moat arrangement



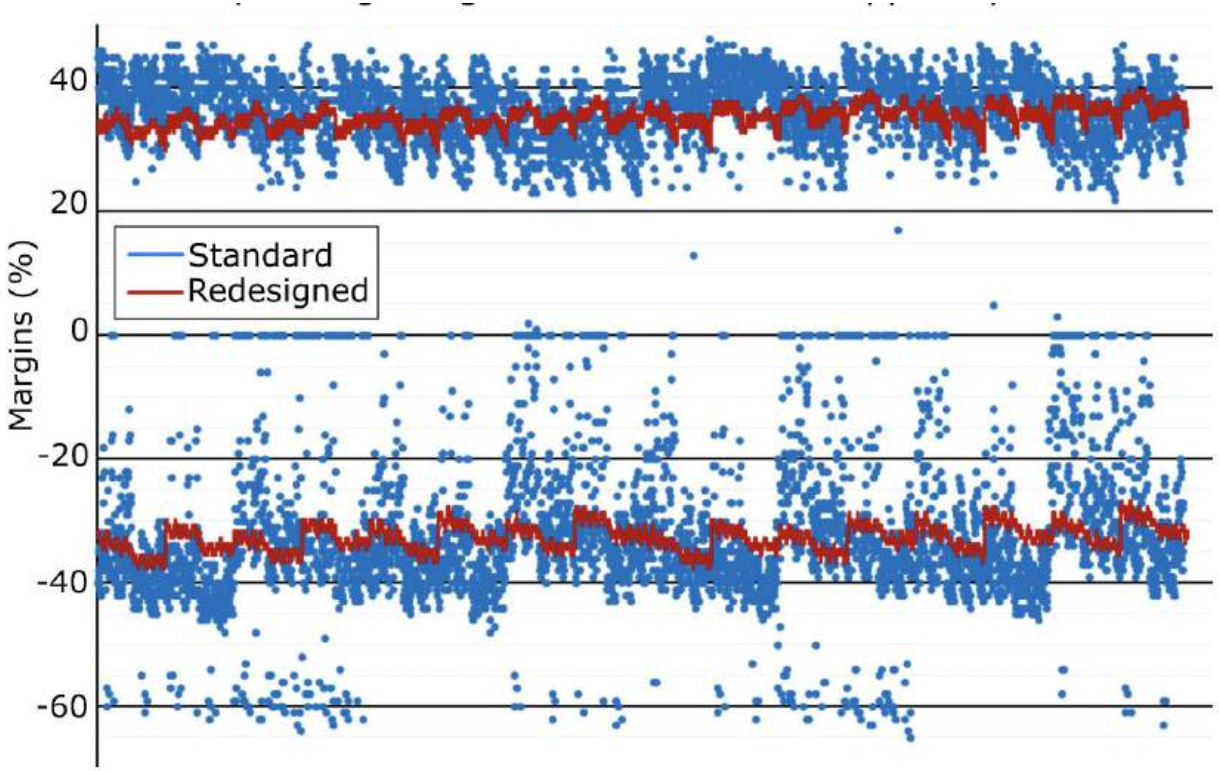
Redesigned moat arrangement



- Move junctions away from moats
- Redesigned transformer with internal moat

Only simulation – experimental validation in progress

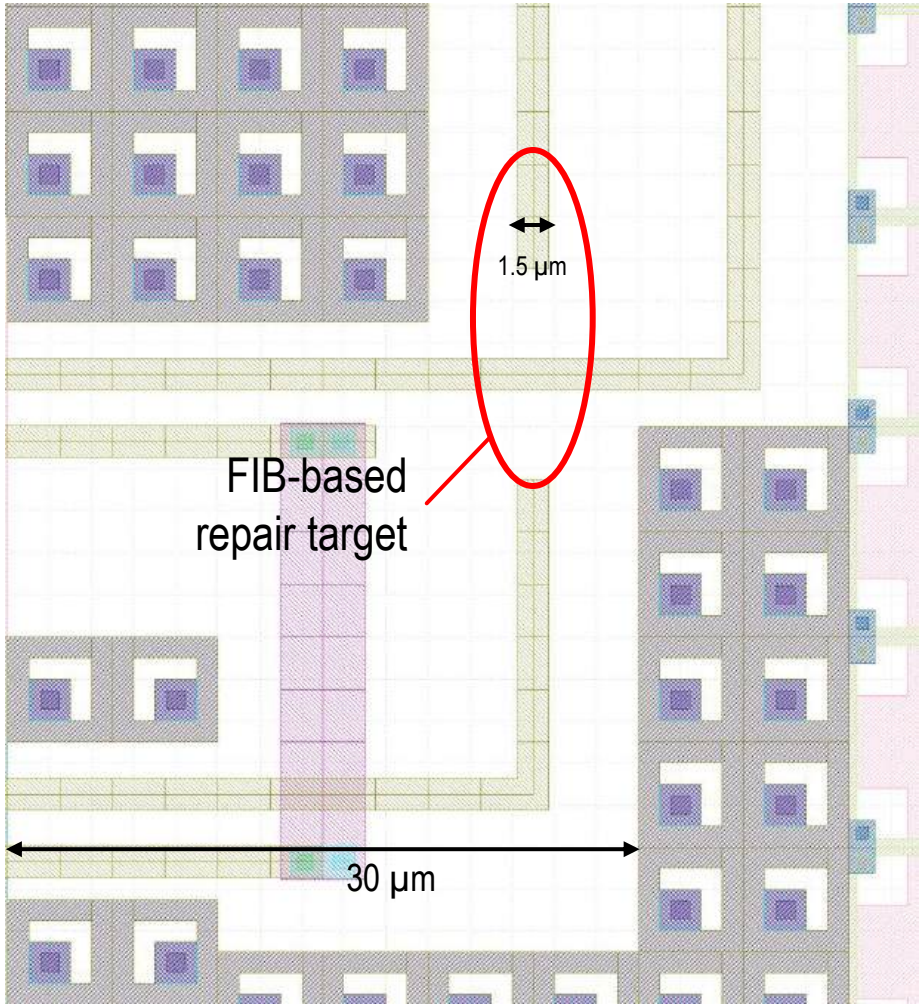
Operating margins of the OR cells with standard and redesigned moat arrangements



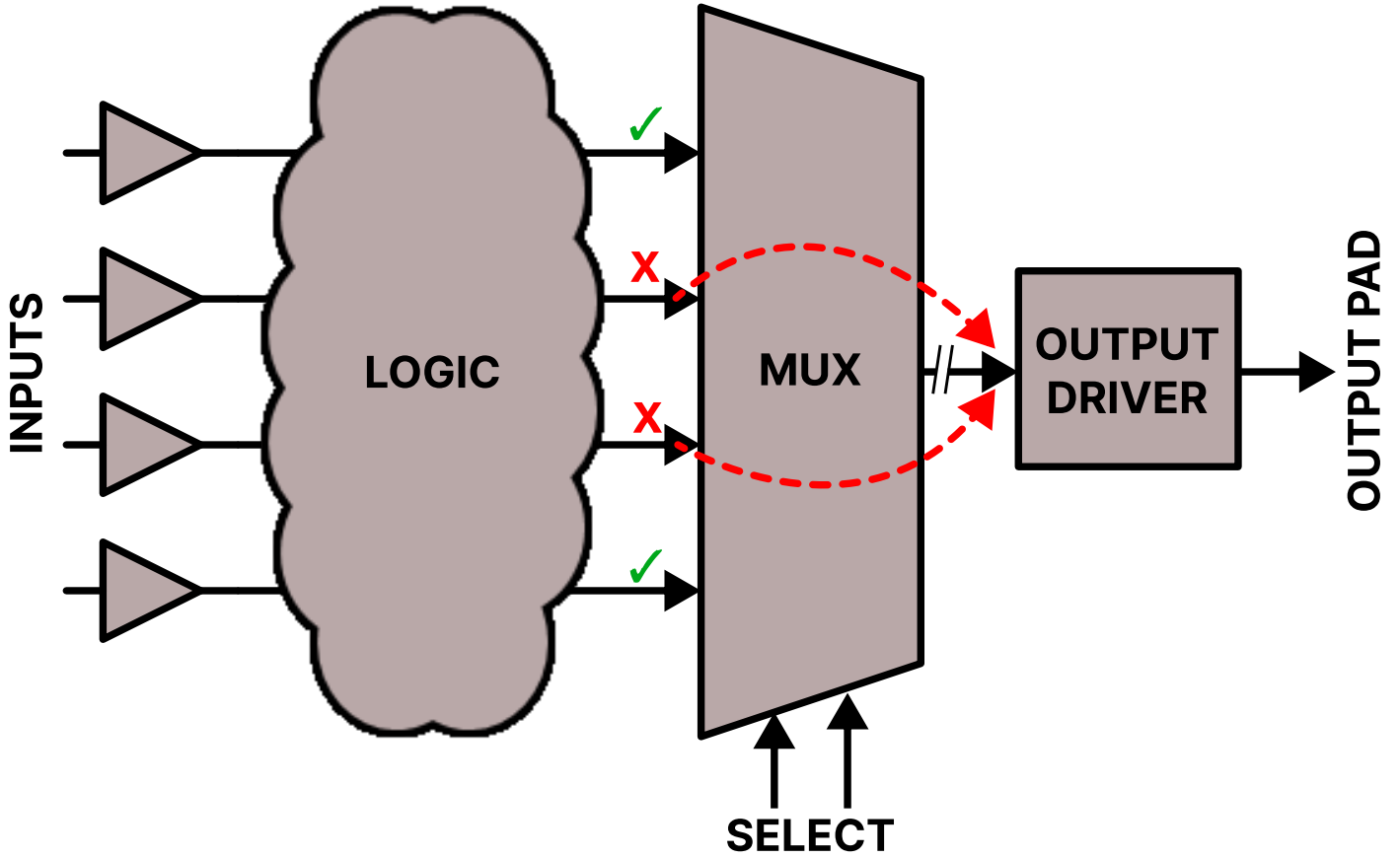
x-axis represents the 4096 possible trapped fluxon configurations in terms of a 12-bit binary sequence to represent fluxons trapped in moats F1 to F12.

L. Schindler *et al., IEEE Trans. Appl. Supercond.*, 2024

FIB Circuit Edit Examples



Design error in ac network of AQFP circuit – FIB-based circuit edit used to repair disconnected line

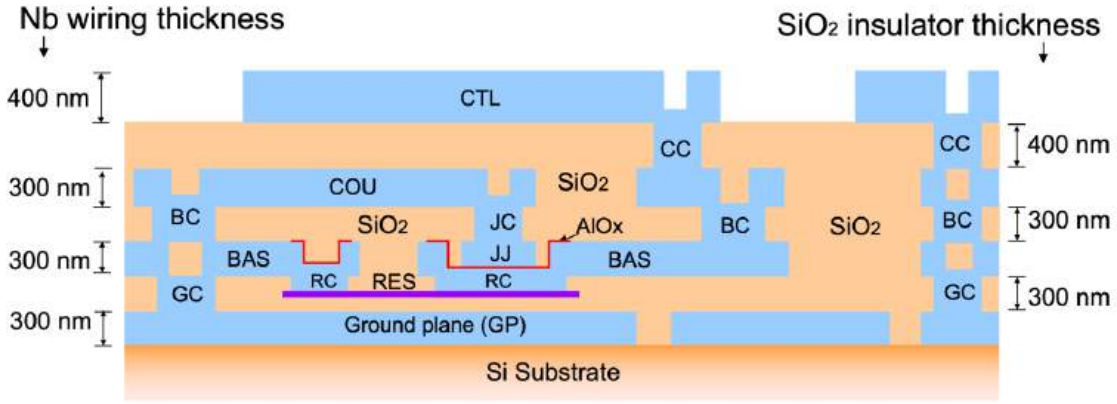


Typical logic test circuit with MUX to select which logic output to observe on single output pad – FIB-based circuit edit used to troubleshoot logic errors from MUX failure.

Microscopy used to pinpoint if failure is possibly due to flux trapping. FIB used to create additional post-fabrication moats to improve operation.

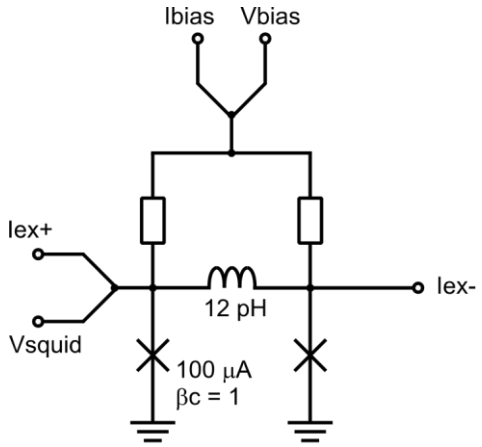
Current progress: SQUID design for flux trap measurements

Cross section of AIST process

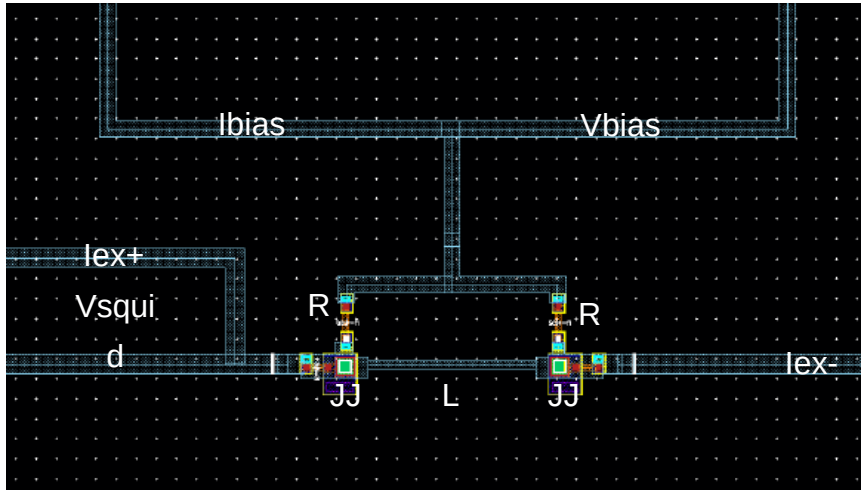


HSTP (J_c = 10 kA/cm^2)
1KP (J_c = 1 kA/cm^2)

Schematic and layout of 1KP SQUID design

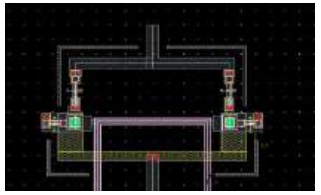


- I_c = 100 μA
- symmetric DC-SQUID

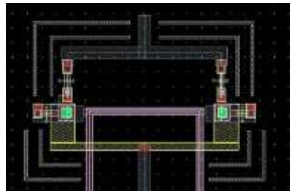


Current progress: SQUID design for flux trap measurements

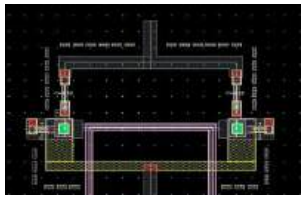
22 types of SQUIDs with different moat structures



1. Pre-moat
2. No moat
3. w+//4.w++
5. d+//6d++

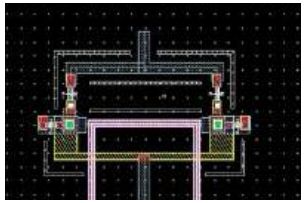


7. 2-layer

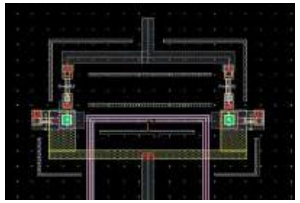


8. Point moat

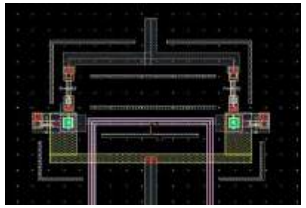
9. 2-layer point moat
10. 2-layer W+
11.Point moat y



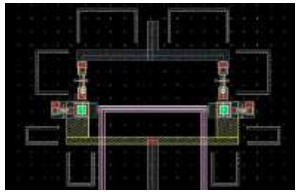
12. in-moat



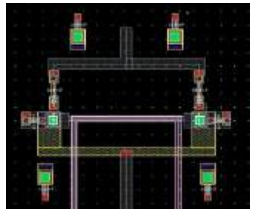
13. inmoat2



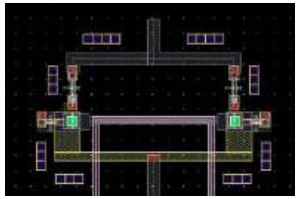
14. Only in-moat
15.Only in-moat2
16.in-moat point



17. U-moat
18. U-moat d-
19. U-moat in
20. U-moatin 2

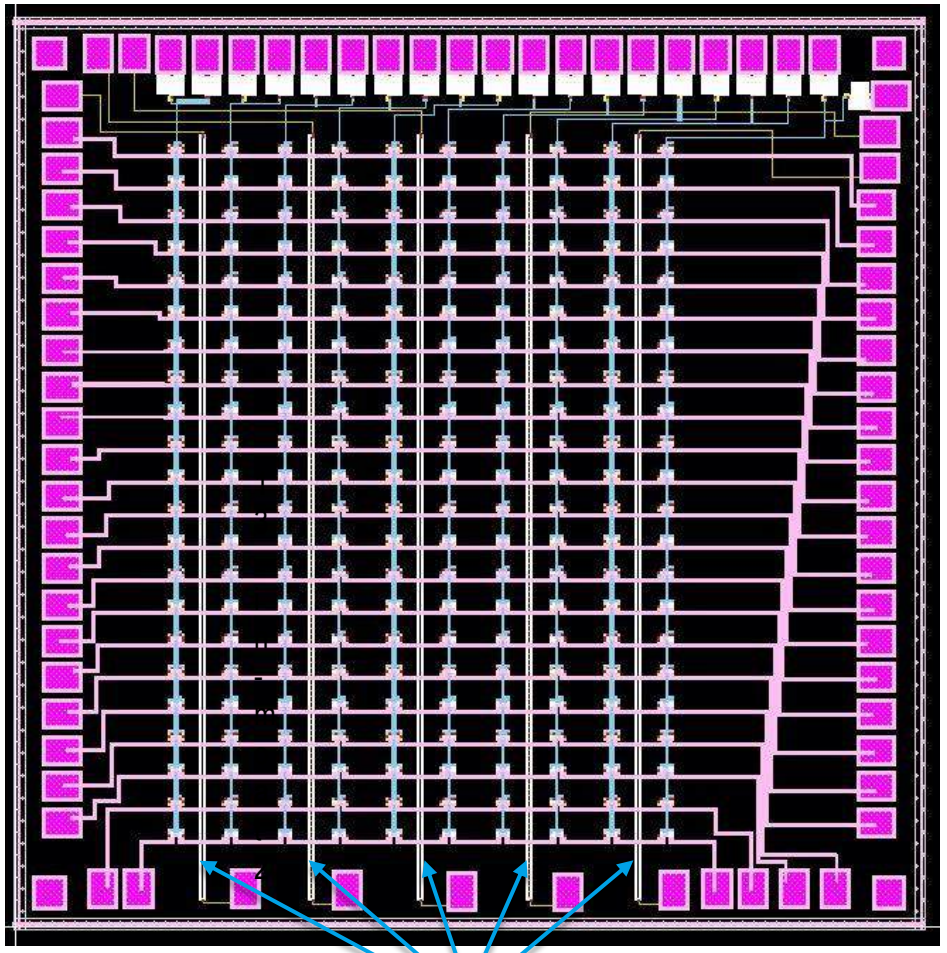


21. JJ moat



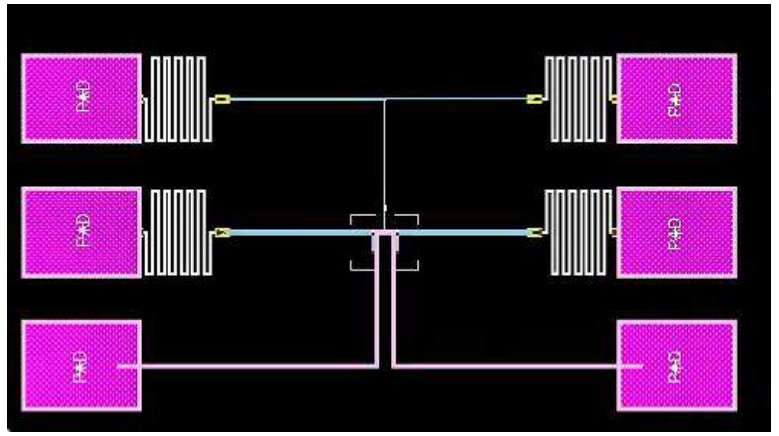
22. JC moat

1KP Chip design with 220 SQUIDs

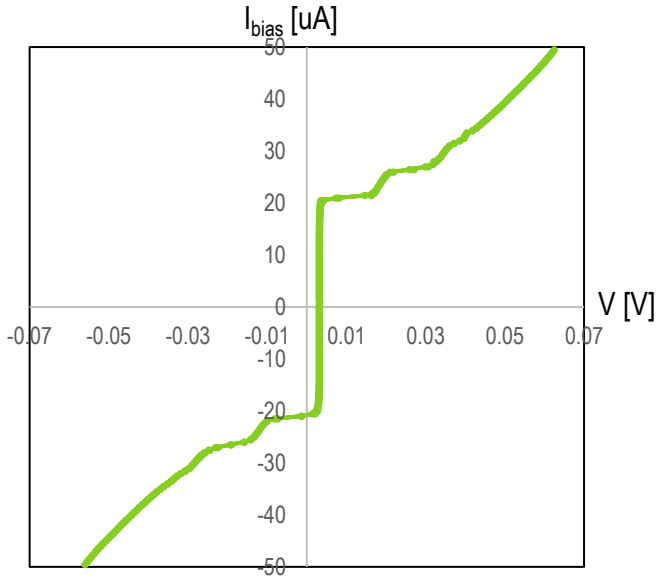


Resistors for creating a temperature gradient

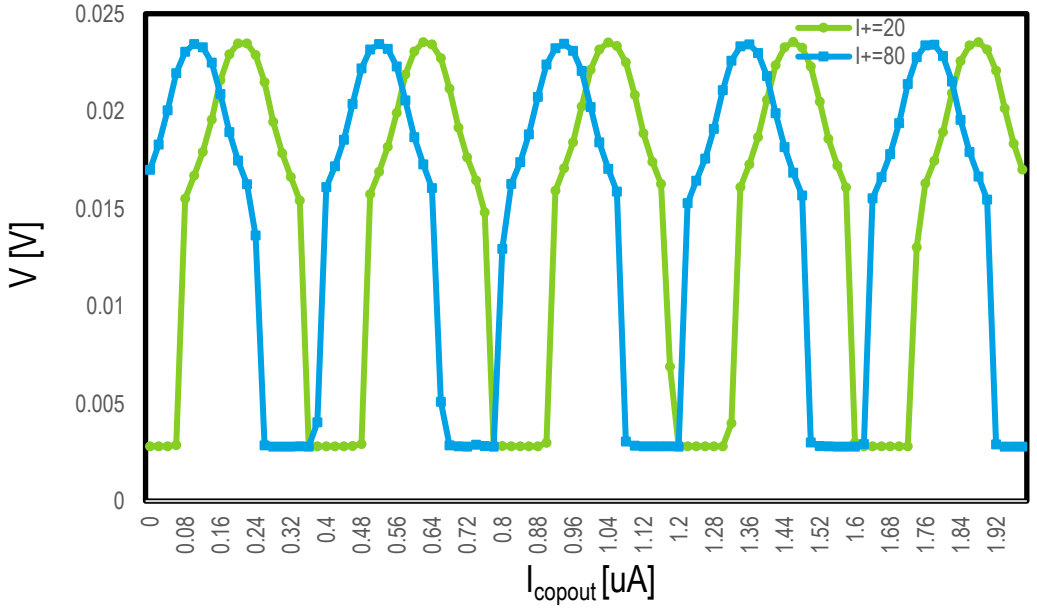
Current progress: SQUID measurement results



IV Curve

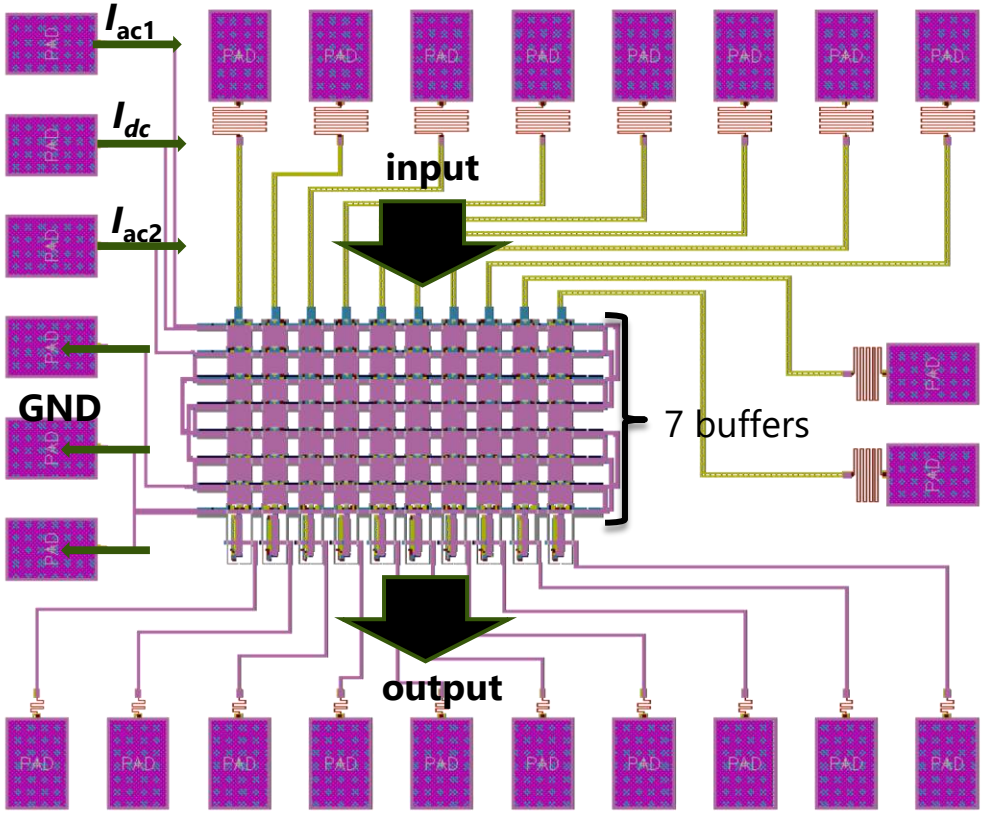


V-Φ Curve

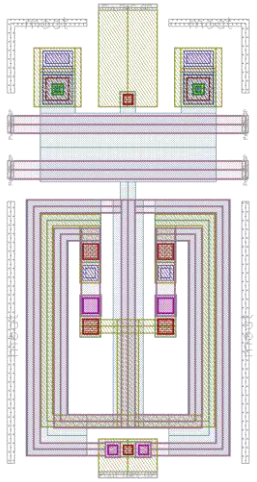


Current progress: AQFP shift registers for flux trap measurements

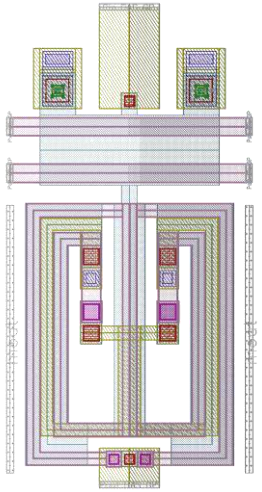
Layout of 10 AQFP shift registers for HSTP



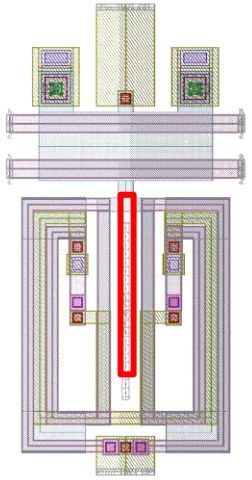
AQFP shift registers with different moat structures



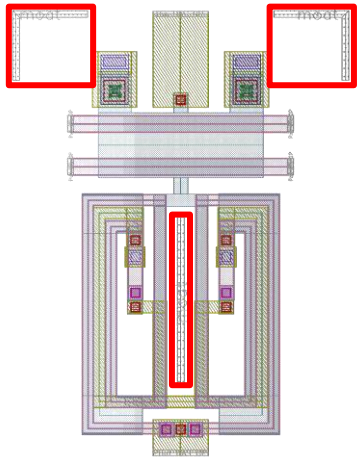
Reference



No moat around JJ

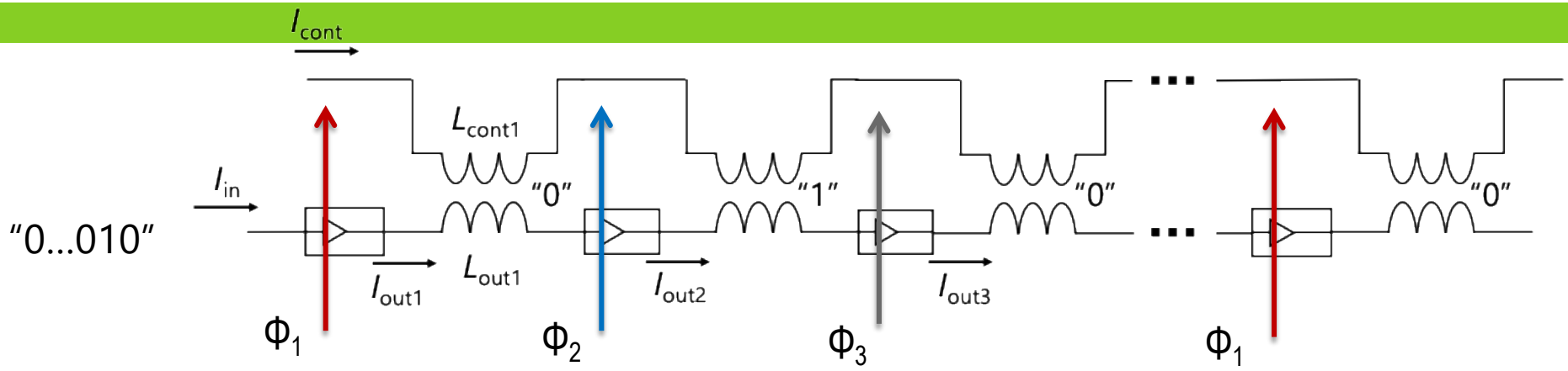


Center moat



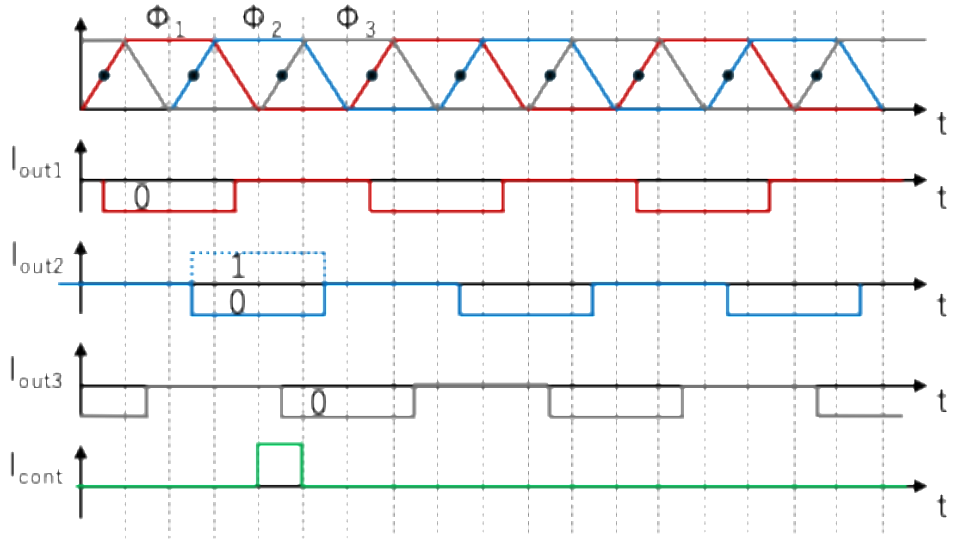
Center moat and far-JJ moat

Current progress: AQFP shift register for individual flux trap measurements



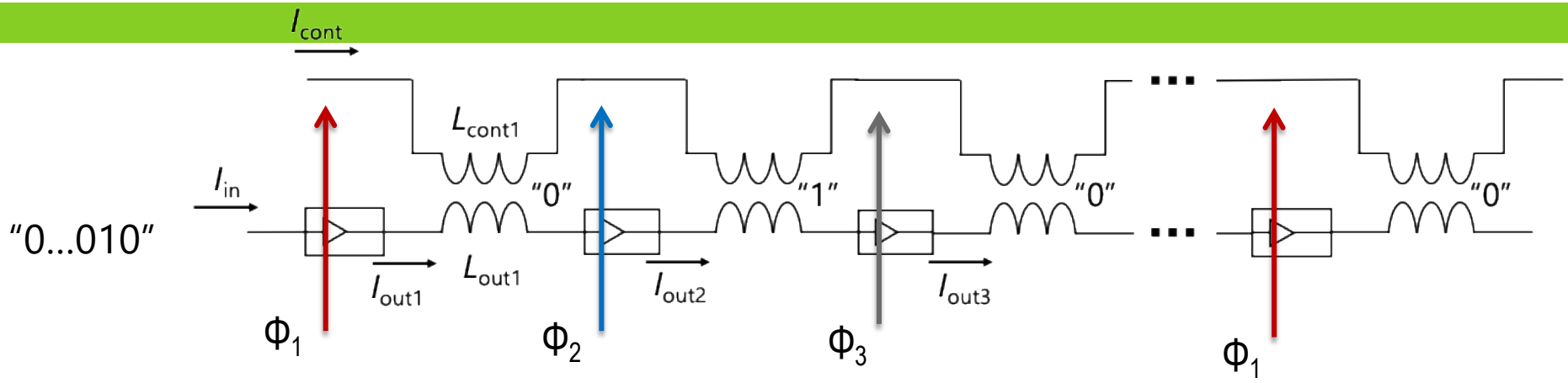
AQFP shift register for individual flux trap measurement

- Only one "1" is sent to the shift register. All others are "0".
- I_{cont} is applied, and the value of I_{cont} at which the "1" output reverses to "0" is measured.
- Similarly, measure the value of Icont' where the "0" output flips to "1
- Derive offset from I_{cont} and I_{cont}' values
- Measured similarly for all buffers

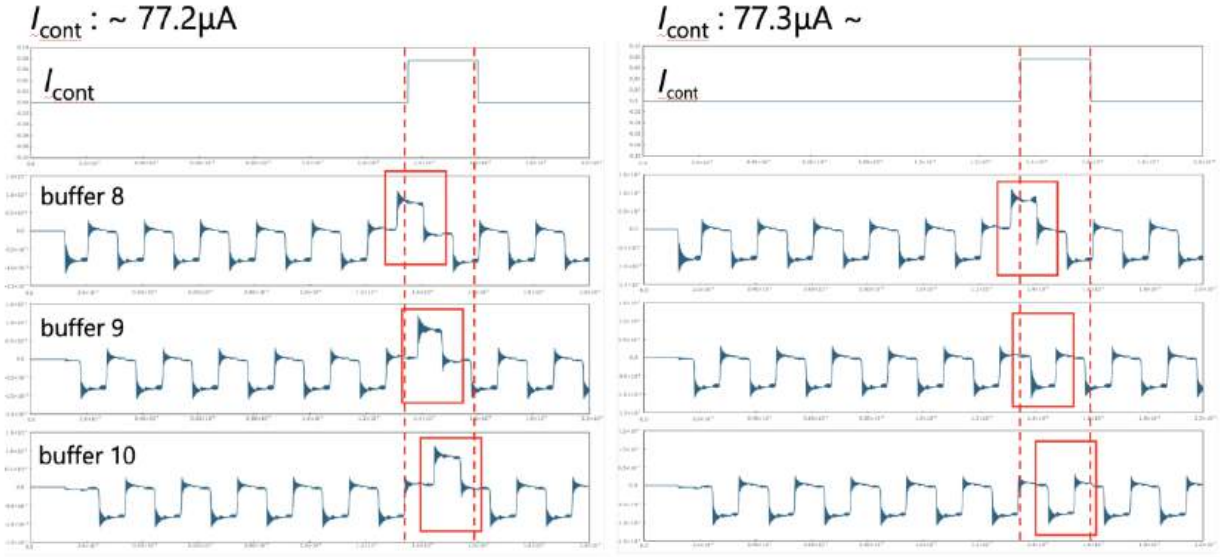


Logic Signals and Timing

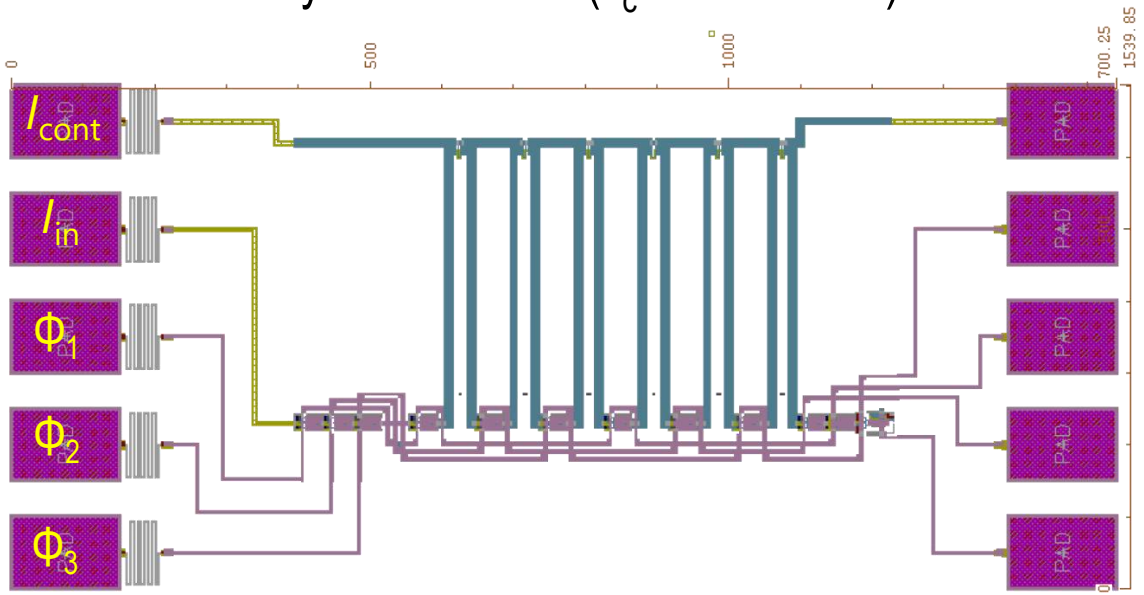
Current progress: AQFP shift register for individual flux trap measurements



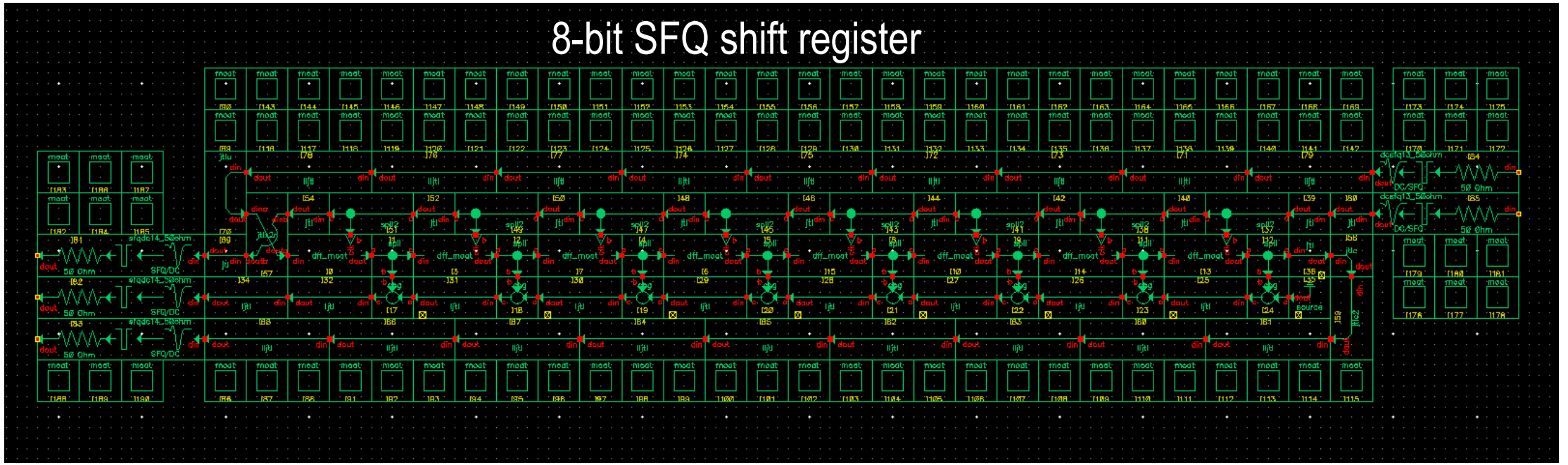
Circuit simulation results



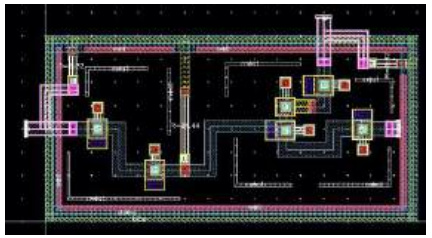
Layout for HSTP (J_c = 10 kA/cm^2)



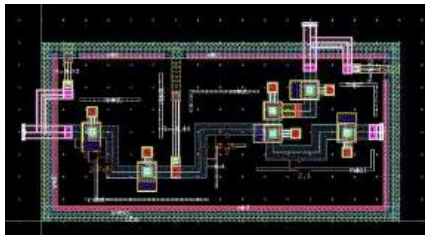
Current progress: SFQ shift register design for flux trap measurements



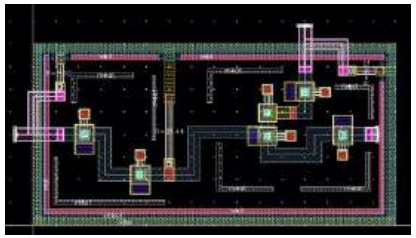
SFQ-DFF with 6 different moat structures



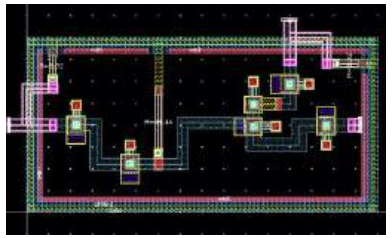
HSTP cell library



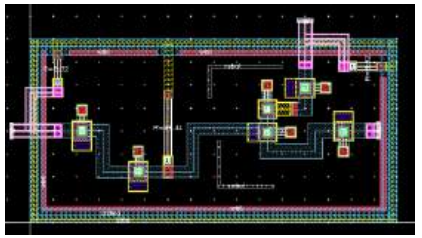
Reduced distance



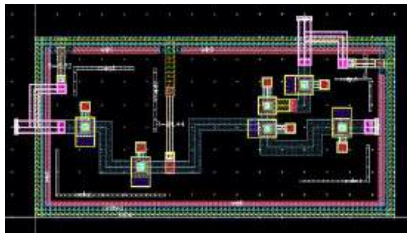
Increase width



No-moat



Storage-loop moat

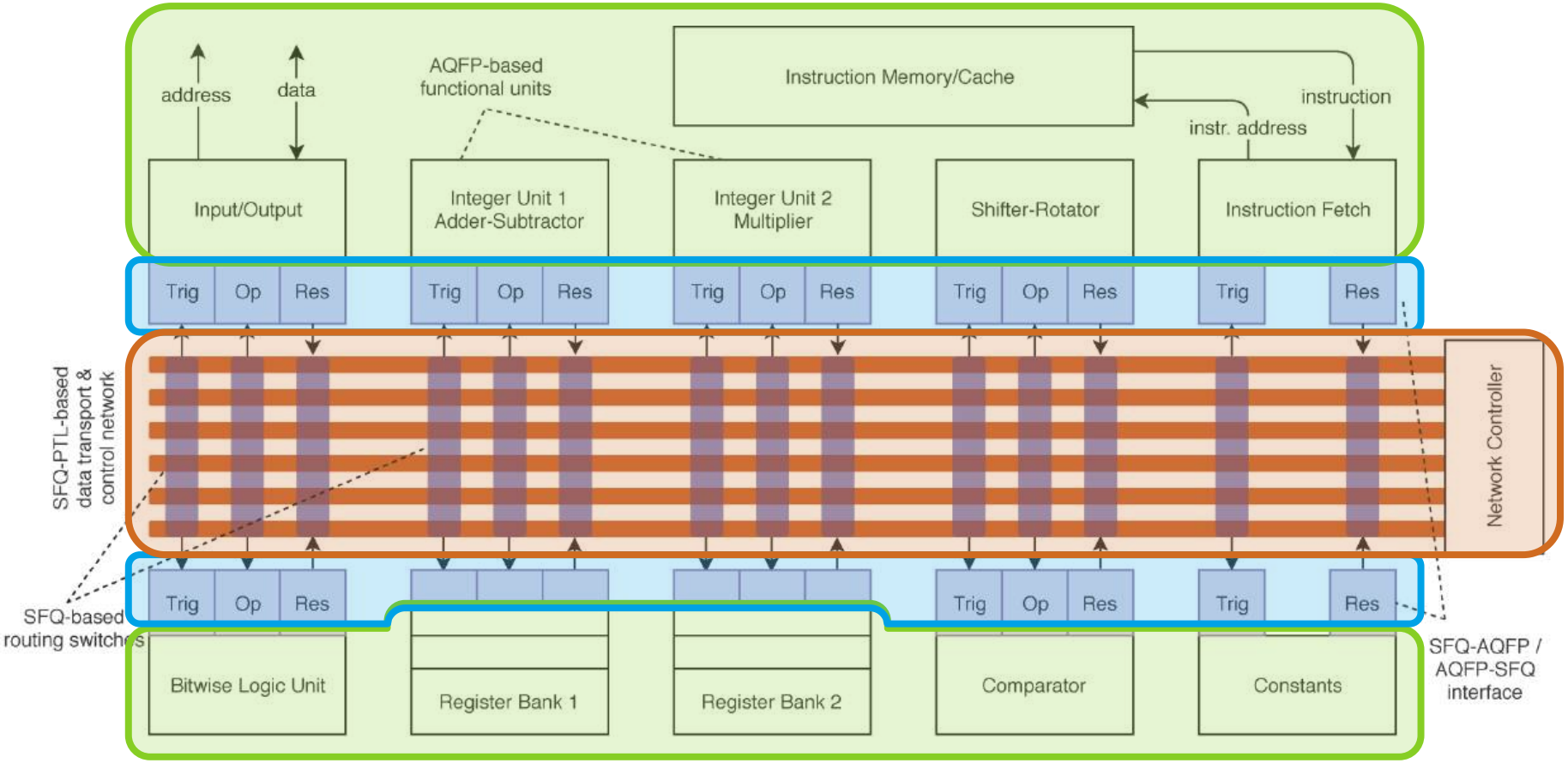


in/out port Moat

Similar circuits will be done for MIT LL 8-Nb layer SFQ5ee process

And if we solve (or meaningfully mitigate) foundational challenges in superconducting digital logic?

Hybrid RSFQ-AQFP Transport Triggered Architecture (TTA)



- Leverage strengths of RSFQ & AQFP [1]
- Globally asynchronous, locally synchronous
- TTA [4] shown to have performance and power advantage in post-quantum cryptography applications over RISC-V

AQFP circuits: TTA execution units and distributed registers

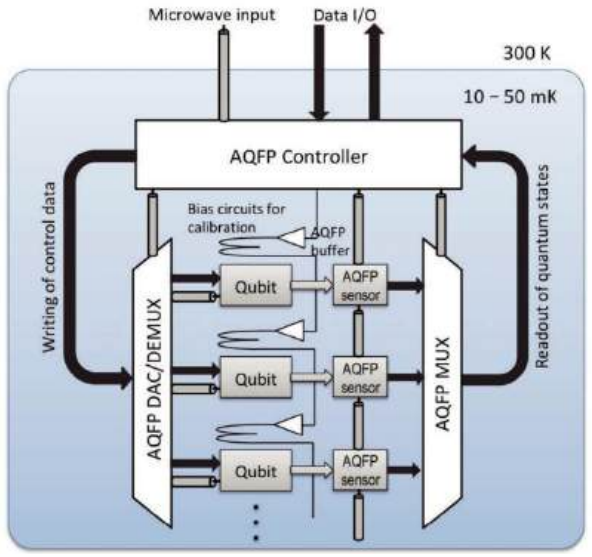
SFQ<->AQFP interfaces: Interface between SFQ/AQFP circuits, SerDes [2]

SFQ circuits: Long distance interconnect network and routing [3]

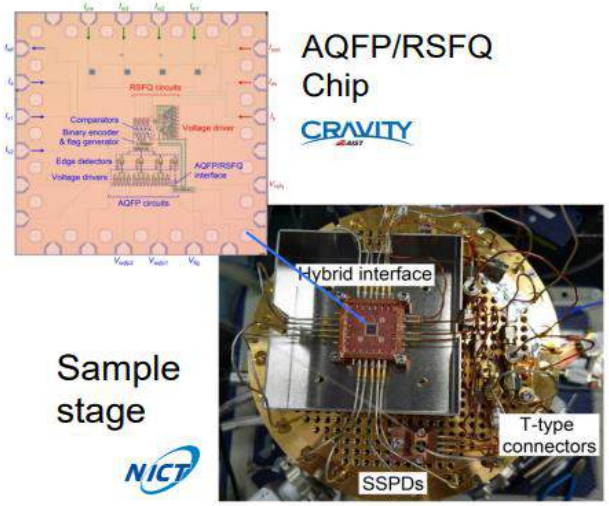
More investigation needed for hybrid design of large-scale RSFQ-AQFP systems.

[1] C. L. Ayala, in *Superconducting SFQ VLSI (SSV)*, 2015/2019 [2] Y. Hironaka *et al.*, *IEEE Access*, vol. 10, 2022. [3] A. Fujimaki *et al.*, *IEICE trans. electron.*, vol. E97.C, no. 3, 2014. [4] H. Corporaal and P. van der Arend Microprocessing and Microprogramming, vol. 38, no. 1, pp. 53 –60, 1993. [5] L. Akçay and S. B. Ö. Yalçin, 2021, DOI: 10.3906/elk-2003-27

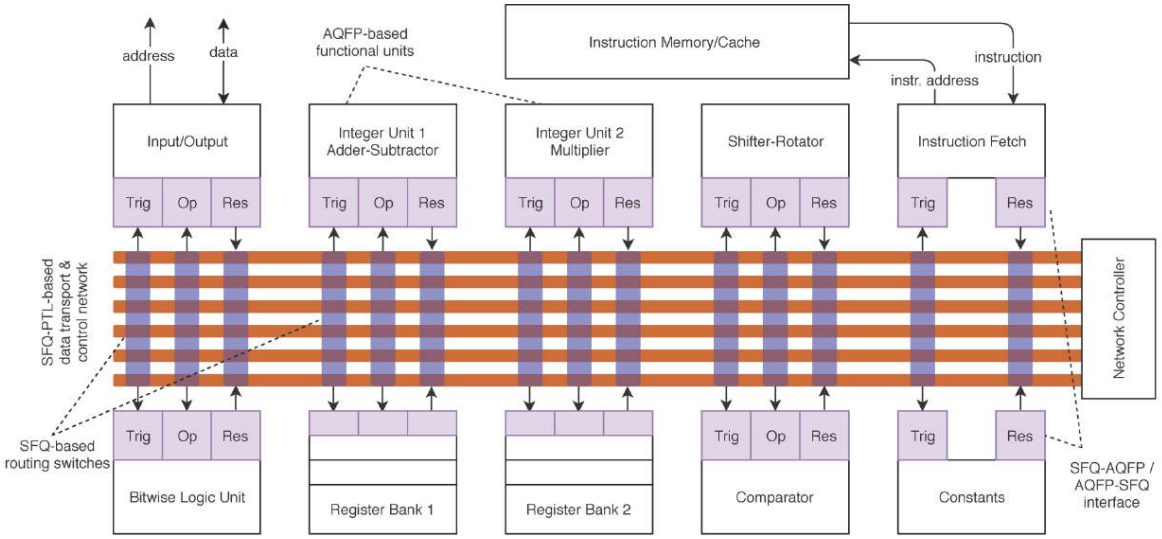
Towards practical applications



AQFP-based QC system concept [2]

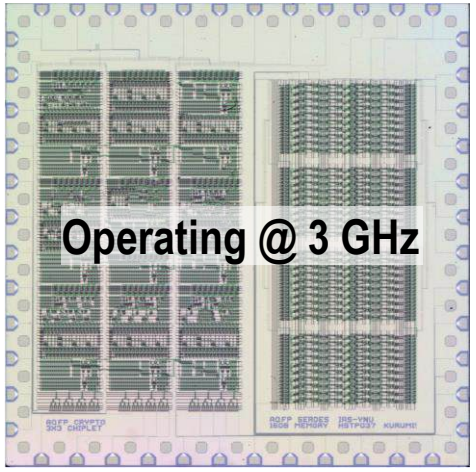


AQFP/RSFQ interface for SNSPDs [3]

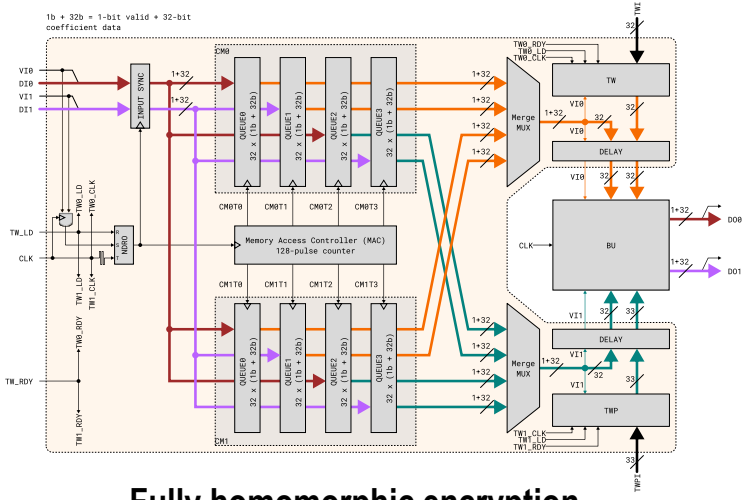


TTA-based general computing / post-quantum cryptography

- Towards 16-bit general purpose microprocessors [1]
- Quantum computing systems [2]
- Photon detector systems [3]
- Crypto-accelerators [4] and AI-accelerators [5]
- High-bandwidth communication systems



Large-scale SHA3 AQFP crypto chip (1 cm x 1 cm)



Fully homomorphic encryption

[1] T. Tanaka, *IEICE Trans. Electron.*, doi: 10.1587/transele.2021SEP0001
[2] N. Yoshikawa, *IEICE Trans. Electron.*, doi: 10.1587/transele.2018SDI0003
[3] N. Takeuchi, *Optics Express,* doi: 10.1364/OE.392507
[4] C. L. Ayala, *ISVLSI 2024, doi: 10.1109/isvlsi61997.2024.00106*
[5] O. Chen, *IEEE Transactions on Emerging Topics in Computing*, doi: 10.1109/TETC.2023.3330979

Questions?

Thank You

ACKNOWLEDGMENTS

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The circuits were fabricated in the Clean Room for Analog-digital superconductiVITY (now Qufab, Superconducting Quantum Circuit Fabrication Facility) of the National Institute of Advanced Industrial Science and Technology (AIST) using the high-speed standard process (HSTP) and low-Jc process (1KP).